LIGHT-HARVESTING PHOTOVOLTAIC CHARGER–SUPPLY MICROSYSTEMS

A Dissertation
Presented to
The Academic Faculty

by

Rajiv Damodaran Prabha

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2018

LIGHT-HARVESTING PHOTOVOLTAIC CHARGER–SUPPLY MICROSYSTEMS

Approved by:

Dr. Gabriel A. Rincón-Mora, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. James Stevenson Kenney
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Ajeet Rohatgi
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Doron Lubinsky
School of Mathematics
Georgia Institute of Technology

Date Approved: [Dec. 07 2017]

To my family

ACKNOWLEDGEMENTS

I would first like to thank my advisor Dr. Gabriel A. Rincón-Mora for his able guidance, emphasis on intuitive thinking and pursuit of excellence that made this research possible.

I also offer my gratitude to the dissertation and proposal committee members for their valuable feedback that helped improve this research.

I want to specially thank my colleagues at the Georgia Tech Analog, Power and Energy Lab for the day-to-day discussions and technical feedback.

I wish to acknowledge the help of Mr. Patrick O'Farrell, Mr. Paul Emerson, Dr. Rajarshi Mukhopadhyay, Dr. Orlando Lazaro and Texas Instruments for their feedbacks, support and for fabricating the prototyped ICs.

I also wish to acknowledge the help of Tasha Torrence from Georgia Tech ECE Department office all through the PhD program.

I would like to extended special thanks and gratitude to my family members and especially my parents for being supportive and patient throughout the program.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

RESEARCH OBJECTIVE

Advances in the semiconductor industry have made possible integration of sensors, processer, memory, and radio transceivers into a small space in the form wireless microsensor nodes. The microsensors when deployed standalone in human body, or networked across hospitals, factories, fields, and others, can save lives, energy and money. However powering the sensors over long period is challenging, as tiny on-board batteries, these sensors can accommodate, store limited energy and replacing the batteries is difficult owing to replacement effort and cost. Fortunately, the environment provides various sources of energy in the form of light, motion, heat, RF, and electrochemical potential, which tiny transducers can harvest to continually supply energy, and extend the energy lifetime of the sensor indefinitely. Among the ambient sources of energy, sunlight when harvested with photovoltaic (PV) cells provides two orders of power greater than other sources.

The driving motivation for this work is that, although sunlight can output 10 to 100 times more power than motion, heat, and radiation, a millimeter PV cell can only capture a small fraction of light, and if that light is artificial, power can be 10 times lower. So with only 10-150 uW available, supplying a few milliwatts of load power requires assistance from a battery. Still, a small battery cannot supply milliwatts for long, so drawing more power from the PV cell and reducing power losses in the system are paramount. Most PV systems today charge a battery from which a power-supply circuit draws power to energize a load. This is inefficient because transferring power twice, to the battery and then to the load, suffers two transfer losses and requires two bulky inductors and two

controllers, which is difficult for microsystems to accommodate. Even the state of the art single-inductor charger-supplies use bulky inductors and cannot robustly draw power from both PV cell and battery simultaneously.

The objective of the proposed research is to study, explore, develop, design, simulate, fabricate, build, test, and evaluate a low-loss CMOS charger-supply photovoltaic (PV) system that draws power from a millimeter PV cell and assistance from a tiny battery to regulate and supply a milliwatt microsystem and recharge the battery. For this, the research aims to (i) to reuse the CMOS technology already available to fabricate circuits to build PV cells and explore which millimeter CMOS cell configuration generates the most power, (ii) to study and evaluate the performance of power transfer circuits available in literature and identify the one that can deliver maximum power from tiny PV cells while incurring minimum losses (iii) to understand and propose how to design the efficient charger–supply circuits (iv) study and design a compact, robust and low-loss millimeter scale single-inductor system that draws PV and assistance from battery to supply a load and recharge the battery with excess PV power , (v) understand how to transfer power between the inputs and outputs with the least amount of losses and (vi) investigate how to do all this while at the same time supplying and adjusting to a vastly variable load quickly and reliably.

SUMMARY

Wireless microsensors not only enable miniaturized applications, like biomedical implants and remote monitors, but can also add intelligence to expensive, previously inaccessible, and difficult-to-replace technologies of scale, like industrial power plants and farms, that improve performance, save energy, and extend operational life. The driving challenge with these devices is limited space because small batteries, for example, store little usable energy, and replacing or recharging a battery requires prohibitively expensive recurring personnel costs. Harvesters circumvent this basic space and cost challenge by continually harnessing energy from the surrounding environment. Of available sources (like thermal, mechanical, magnetic, chemical, and light), solar light produces the highest power density, and although indoor lighting is not as rich, thermal and magnetic sources produce even lower power densities and mechanical and chemical transducers are difficult to integrate. Nevertheless, for a millimeter scale microsensor the area of light exposure is small and therefore harvestable power is low even for solar light and much smaller for indoor conditions. As a result the charger–supply systems that transfer these low power levels have to be efficient. This at low power levels is difficult as the power transfer circuit might itself consume most of the power. Switched-inductor power transfer circuits provide higher conversion efficiency in comparison with the switched-capacitor counter parts; however they generally use bulky inductors that occupy large volume. Therefore to achieve high efficiency and power density the charger–supply power stage can use no more than a single millimeter scale inductor, input and output capacitors as external passives. Nevertheless achieving high efficiency with millimeter

scale inductors that have large series-loss incurring parasitic-resistances is extremely challenging.

With respect to the state of the art, compared to fuel cells, motion based harvesters and heat-driven generators, photovoltaic (PV) cells, which are essentially pn-junction diodes, produce higher power levels from solar light and integrate more easily into CMOS technologies. Still, millimeter scale PV cells can produce only around 150 μW from sunlight and few microwatts in indoor lighting condition. In a wireless microsensor, transmission events can use milliwatts of power, but these events seldom occur and sensor is mostly idling or in sensing mode, which burn nWs power. This allows envisioning a system, which relies on battery-assistance to supply high power events and harvest energy to supply the load and charge the battery at other times. Most PV systems (chargers) today charge a battery from which a power-supply circuit draws power to energize a load. This is inefficient because transferring power twice, to the battery and then to the load, suffers two transfer losses and requires two bulky inductors and two controllers, which are difficult for microsystems to accommodate. The CMOS switched-capacitor chargers avoid the bulky inductors but on-board capacitors can carry and transfer only few microwatts of power while losing most of the power it transfers. The charger-supply circuits reuse the same power stage to supply the load and charge the battery and as a result deliver more power for the same volume. Still, the integrated switched capacitor charger–supply systems can transfer only small power levels and that too inefficiently. The single switched-inductor charger–supply circuits are more promising but the state of the art circuits use bulky low-parasitic-resistance inductors that

occupy large volume and inefficient power transfer schemes that losses most of the power they harvest.

The objective of the proposed research is to therefore (*i*) investigate the limitations of the state of the art; (*ii*) design, develop, fabricate, test, and evaluate an efficient micro-power integrated light-energy harvester-charger circuit. For this, the research aims are (i) to reuse the CMOS technology already available to fabricate circuits to build PV cells and explore which millimeter CMOS cell configuration generates the most power, (ii) to study and evaluate the performance of power transfer circuits available in literature and identify the one that can deliver maximum power from tiny PV cells while incurring minimum losses (iii) to understand and propose how to design the efficient charger–supply circuits (iv) study and design a compact, robust and low-loss millimeter scale single-inductor system that draws PV and assistance from battery to supply a load and recharge the battery with excess PV power , (v) understand how to transfer power between the inputs and outputs with the least amount of losses and (vi) investigate how to do all this while at the same time supplying and adjusting to a vastly variable load quickly and reliably.

For harvesting light energy this work reuses the low cost single-well CMOS technology that fabricates the circuits to implement the PV cell, Chapter 2. This research implemented and compared the possible CMOS PV cell options in a single-well CMOS technology and proved harnessing power using the P^+ in N well top junction harnesses only 20% of the total energy that both the P^+ in N well junction and N well in substrate junctions can harness together. The research also proposed the configuration that opens the P^+ terminal to combine the shallower and deeper junctions while eliminating one top-

surface metal connection from the structure, so more light can penetrate to generate even more power. Even though top junction only PV cell can isolate and accommodate multiple PV cells and circuits in the same die, it is normally undesirable. Since microsystems can only avail a few millimeters, dedicating one die to the PV cell and stacking it above the CMOS circuit produces much more power than placing the PV cell alongside the circuit. The study also revealed stacking PV cells are inefficient due to parasitic substrate leakage losses. Therefore this research proposes and uses a single open P^+ in N well CMOS PV cell as the transducer to harness light.

To identify the power stage that can transfer the most amount of power from a tiny on-chip PV cell, the research compared the switched-inductor and switched-capacitor circuits while transferring similar power levels, Chapter 3. To maximize harvested output power, the circuit should be efficient, which is to say it should transfer and condition power by switching an in-package inductor. Still, Ohmic losses P_R are dominant and proportional to P_{PV}, with controller quiescent power P_Q not far behind and gate-charging losses P_G further back. Interestingly, capacitor-based circuits consume more power because they conduct higher RMS currents. Moreover, on-chip implementations lose additional power in charging and discharging parasitic bottom-plate capacitors. In other words, switched-inductor harvesters harness more light energy from chip-sized PV cells than switched-capacitor circuits, which is especially important when P_{PV} is low, cloud cover and artificial lighting conditions persist, and unobtrusiveness (i.e., integration) is imperative.

This work further compared the two prominent single-inductor charger–supply topologies, non-reversing and reversing, and identified the supply voltages, switch

implementations, and inductor sizes which favor one topology over the other. This work shows how to design low-loss battery-assisted photovoltaic-sourced CMOS charger–supplies. And that non-reversing switched inductors are less lossy than the reversing counterparts when the output voltage is greater than the battery voltage, and *vice versa* otherwise. Headroom, dead-time currents, and reverse-current protection dictate which and how FETs should switch the network. Unidirectional switches that conduct dead-time currents in the same direction can be diodes or diode-emulating FETs. But as inductor resistance and losses climb, the benefits of low-loss CMOS choices diminish. In these cases, switches can be more lossy, and as such, occupy up to 80% less silicon area.

A millimetre scale photovoltaic cells can provide only around 100 µW of power even in direct sunlight. However the sensor load can draw milliwatts of power while receiving and transmitting data. In the scenario that sensor needs more power than the PV cell the system has to draw assistance from battery to satisfy the sensor load. The automatic mode control proposed in this work identifies monitors load condition to decide when to draw battery-assistance to supply the load and when to charge the battery with excess PV power. This way favours single energy transfer from PV cell to load and drawing battery energy only when required. This work further showed that interleaving PV packet with a variable size battery packet can simultaneously draw power from PV cell and assistance from battery to satisfy the load. Unlike state of the art clocked systems that interrupt the flow of PV or battery packets to send the other, this method allows for a more robust system that doesn't interrupt the PV or output control loops while transferring power. The uninterrupted flow of PV packets also maximizes the power that

the system can draw from PV cell as any power that PV capacitance stores without being drawn can be lost across the PV diode.

The first prototype in the research implements a fixed energy packet variable frequency control scheme that maximizes efficiency of power transfer from PV cell and load using the traditional 6 switch non-reversing power stage. In the prototype the battery power transfer uses a variable packet size scheme which is inefficient. To improve the efficiency of the battery power transfer, the second prototype proposes a new multiple fixed energy packet scheme, where the circuit provides multiple battery packets in between each PV packets. The multiple battery packet transfer scheme as a result achieve high and near constant efficiency across load power

The maximally efficient multiple battery packet control, 2nd prototype, ensures priority for PV packet transfer and avoids condition where systems interrupts PV loop to send battery packets. The PWM loop that regulates the output during battery-assistance reduces the ripple across the load when higher power more noise sensitive analog blocks turn on. The research studied the different power stages available in literature and improves on the reversing charger–supply circuit in literature by replacing NMOS output switches with PMOS output switches and implementing a new switch sequencing to reduce gate-drive losses. The new switch-sequencing scheme aligns switching action in the reversing circuit to share the ground switch turn on time such that there is only on switching event while transferring a PV and a battery packet unlike literature that requires two. The mode segregating control scheme allows for separation of high power battery-assistance mode and low power heavily sourced mode and as a result lends the power stage to use variable switch size of different modes unlike the state of the art

which uses a single switch size for both transfers. The robust control method and, the duty-cycled control circuits that implement them allows for higher PV frequency and as a result lower input capacitance. In the second prototype using the photovoltaic voltage to set the PV frequency also helps to avoid quiescent power consuming oscillator used in most state of the art.

The first prototype improved the PV transfer efficiency by transferring fixed packet size variable frequency PV packets. Even though the variable sized-battery packets in this schemes incurred higher losses while regulating the output tightly across power levels, this prototype showed 7 times higher performance in comparison to the state of the art. The second prototype improved the battery assistance efficiency by sending multiple fixed energy battery packets in between the variable frequency fixed size PV packets, while ensuring independence of power flow between PV to load and battery to load. This implementation performs 13 times better than the first prototype and 85 times better than the other state of the art. Chapter 4 explain how the controller switches the power stage to draw and deliver power from the PV cell and the battery to supply the load, and when possible, to charge the battery. Chapter 5 presents the CMOS implementation and Chapter 6 present and evaluates the system performance.

CHAPTER 1. ENERGIZING AND POWERING MICROSYSTEMS

Advances in semiconductor and MEMS fabrication technologies have made possible integration of sensors, processor, powering circuits, energy storage and transceivers into a small space [1]–[30]. Recent progresses in low power transfer and management techniques [1]–[10] allow these sensors to be autonomous relying on on-board energy sources as supply for a substantial lifetime. Addressing the twin challenges of small size and low power operation enables autonomous microsensors, also known as wireless microsensor, that can sense and process information thereby adding intelligence to the surroundings, enabling a host of applications. These wireless microsensors can aid in various applications, they can be standalone sensors, for example, biomedical implants sensing body functions or form a network of sensors that adds intelligence to large infrastructure like building, farms, factories, power transmission networks and in military applications.

1.1 Applications

1.1.1 Biomedical Implants

The key features of wireless microsensors are their small size that allows for low cost, portable sensors and low power dissipation that enables autonomous functioning. Implantable wireless microsensors can reduce the number of invasive surgeries by generating power from environment and serving in the human body for a long duration. In biomedical applications, embedded-sensors in the body sense vitals and report periodically and in case of emergencies [1]–[2]. [1] places a wireless intraocular pressure

monitor in the eye to continuously monitor of retina pressure for the treatment of glaucoma. The size of the sensor in Fig. 1.1 is around 1.5 mm^3 and incorporates a capacitive MEMS sensor to measure pressure, thin film lithium ion battery and two integrated circuits (ICs). The top IC contains solar cell, wakeup controller and wireless transceiver and the bottom IC consists of the power management unit, processor, memory and capacitance to digital converter, all enclosed in a biocompatible glass housing. The average power consumption of the sensor is less than 100 nW. Similarly [3] introduces an IC for pacemaker application. The wireless-implantable microsystem in [4] has a micro-fabricated glucose sensor that continuously monitors the blood glucose.

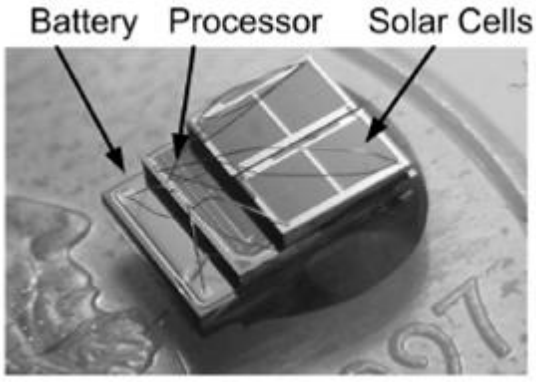


Fig. 1.1 Intraocular pressure sensor [1] © IEEE 2011.

1.1.2 Wireless sensor networks

Wireless microsensors can also add intelligence to large infrastructures [5]–[17]. Typically in such applications millions of sensors form a network, wireless sensor network (WSN), of sensors sense and process data, these sensors communicate with a base station or command center that makes system decisions as in Fig. 1.2. In military application, the WSNs can help in battlefield tactics, target identification, monitoring

soldiers, resource management and enemy recognizance [14]–[17]. Another application for WSNs in utility distribution [11], can enable smart grids that make intelligent decisions to balance resource and demand, as well as managing the power mix of renewables and traditional power. Further WSNs also help in monitoring resource thefts, low hanging conductors, insulation deterioration, and fault detection.

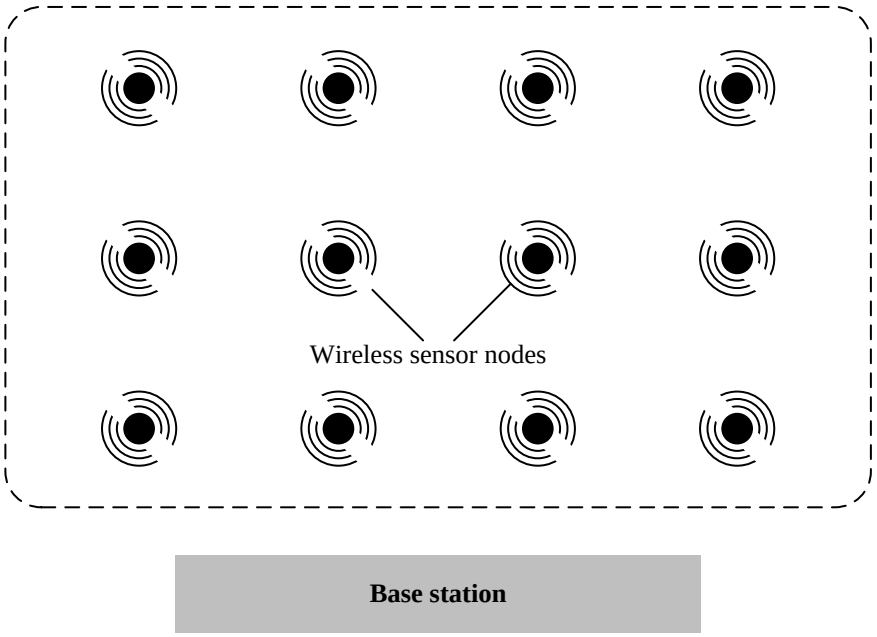


Fig. 1.2. Wireless sensor networks.

Another potential application for the WSNs is in monitoring buildings, for example to monitor the building integrity especially in earthquake prone areas, air quality management, and temperature management [12]. WSNs can also help in environment monitoring, to monitor the flying pattern of birds, monitoring wildlife habitats for protection and studies [13]. It can also help in agriculture to survey microclimates to improve productivity and in produce quality management [13]. It can also add monitoring in industrial process in toxic environment [13], inside machines or air vents. Stock

management in warehouses, shipping containers, grocery stores are other possible application for wireless sensor networks

1.2 Operation

A typical wireless microsensor [1]–[2], Fig. 1.3, primarily consists of sensors, sensor interface, processor, memory, transceiver, powering and energizing sources, and power-flow management IC. Sensors come in a variety of classification that includes temperature, image, MEMS, chemical sensors. CMOS technology can implement the temperature and image sensor using p-n junctions that produce current and voltage, with the thermos-electric effect and photovoltaic effect in response to temperature difference and light. Leakage current or temperature dependent references are good method to measure temperature.

MEMS sensors typical have moving parts that vary the capacitance with respect to an external stimulus. Another method of reading in the mechanical variations is to use piezoelectric material laid out on top of the moving parts; here the stress variation on the material generates a voltage difference as output. In the microsystem the input from the sensors needs to read into the system in form of electrical signals the CMOS sensors naturally generates voltage and currents, however in case of MEMS sensor the capacitance variation have to read into the IC by a sensor interface.

Nevertheless in any case a lower power sensor can only generate a low-level signal, which a low noise amplifier (LNA) has to amplify with good noise suppression to input into the processor. The low noise amplifier engages circuit techniques like chopper stabilization, auto-zeroing and power supply noise rejection to provide a clean signal to

the analog to digital converter (ADC). A low power ADC then digitizes the information of low power digital processing. The digital logic in the processor then evaluates the information with preprogrammed algorithms. Memory, SRAM and DRAM, serve as a cache for processed information, algorithms and predefined date points.

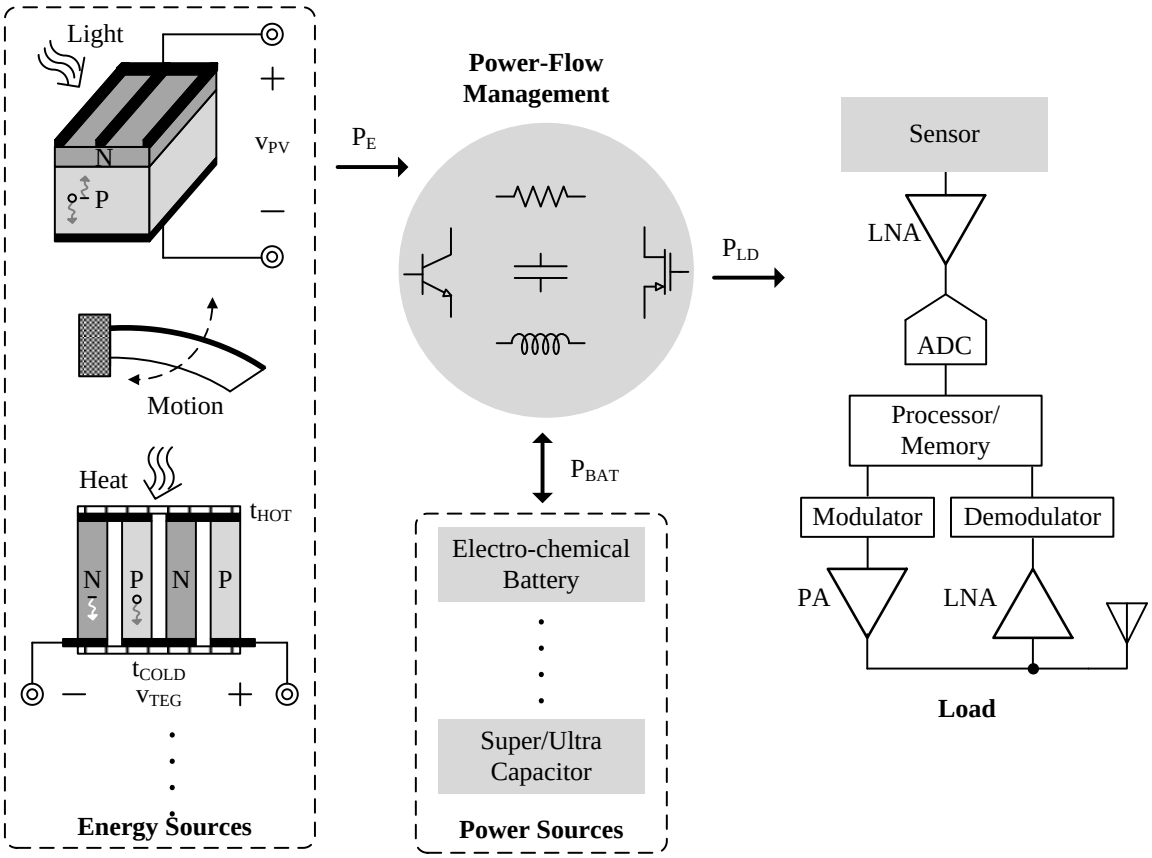


Fig. 1.3. Generic wireless sensor node.

The wireless transfer of the processed information is using CMOS compatible flat antennae. For this purpose the processor encodes the data and sends it out with an appropriate communication scheme. The modulator combines the encoded-data with the carrier signal and input the analog signal to the power amplifier, which further drives the antennae. Similarly the antennae can receive commands from a base station, here an LNA

first amplifies the signal, a demodulator removes the carrier frequency and the processor decodes the digitized command and performs appropriate action.

The processors and sensors consume varying power and at best operate at optimal voltages. The transceiver normally consumes the most power among as the sensor loads. To power these loads one of the system incorporates batteries, super capacitors etc. as option for storing energy. However tiny batteries these sensors can accommodate easily deplete so the system houses ambient energy harvesters that can continually extract energy from the environment and replete the battery. The available power and energy sources as well as the load operates optimally at difference voltage levels and supply and extract varying power levels therefore a power flow management circuit is typically essential in system to ensure an efficient functioning of the sensor.

1.3 Powering Requirements

The focus of this research is to efficiently power the micro sensor to increase its functional life. For this it is important to evaluate the power consumption of sensors, processor, and transceiver in the system.

1.3.1 Sensing

The sensors are typically always on blocks in the system as a result they should potentially consume least amount of power for ensuring low supply life, table 1.1. The CMOS temperature and image sensors in its CMOS implementation can consume as low as 100s of nWs. [18] presents a temperature sensor operating at 0.5 V and consuming 250 nA. Similarly an image sensor in [19] consumes only 140 nJ per frame for a 128 × 128

image sensor. The lower limits of the sensor power is generally set by the parasitic leakage and noise that limits the minimum sensor output and power to hold sampled values.

Table 1.1 Power requirements

Modes	Active Power
Idle	20 nW – 1 μW
Sensing & Processing	80–150 μW
Reception	0.2–0.9 mW
Transmission	0.3–7 mW

1.3.2 Processing

The wireless microsensor has to incorporate processing and data storage on-board as the frequently sending sensed-data lead to large transmission loss and data congestion. The processor generally consists of the digital logic than implement processing units and memory to store algorithms and data. The selection of technology is important for optimal low power operation, the shorter CMOS technologies have lower threshold voltage v_{TH} and therefore lower supply voltages v_{DD} resulting in lower dynamic power. However lower v_{TH} leads to higher subthreshold leakage for off state switches. Therefore, if the on duty cycle of the processor is larger smaller technologies are optimum and reverse is true if the off time is the larger portion. Voltage scaling is another technique to reduce losses, lower voltages leads to lower leakage power and dynamic power, however the delay increases. The major design focus in voltage scaling is the trade-off between performance and power consumption. The larger delays can increase the leakage power proportion with respect to dynamic power. The optimum supply voltage for sub-micron technologies are around 0.6 V. In the memory design the leakage power is of a larger

concern as larger leakage can affect data integrity. The choice between SRAM and DRAM is based on the robustness and power consumption [1]. The cell design memory is another variable in lower design trade-off between robustness and higher leakage power.

1.3.3 Transceiver

The transceiver circuits consist of the oscillator, power amplifier, low noise amplifier and modulating/demodulating circuits. The miniaturization of the antennae is one of the challenges in reducing the sensor size. The smaller antennas and lower frequencies lead to higher losses and lower efficiencies. The operation of circuits in weak inversion can reduce the power consumption of the transceiver circuits. In [1] the receiver consume considerably less power operating at 0.6 V. the oscillators that supply in GHz-carrier for better antennae efficiency can be quite power consuming, some of the recent low power techniques include using MEMS resonators in oscillator. The choice of the radio architecture also aid in reducing the power levels [20]–[25], the ultra-wide band (UWB) receivers that transmit the narrow pulses of energy can lower energy consumption. UWB can also have an all digital implementation and lower wake up time.

Back scattering radio architectures also reduce the on-board energy consumption of the sensors. In the back scattering radios the power transmitter base station can transmit the data to the sensor and sensor communicates by changing the antennae impedance and reflecting the signal back. As a result, the back scattering radios do not need power hungry power amplifiers. The system level techniques to reduce power consumption include sensor placement to reduce distance of transmission and duty

cycling to reduce the frequency of data transmissions. The heavy duty cycling can severely reduce average power consumption even when active power consumption is quite high. There are several schemes to wake up the transceiver. The more prevalent is the periodic waking up where a local oscillator can trigger the transmission periodically however this might lead to unnecessary communication as well as delayed response in emergencies. The event triggered control however solves this issue by sensing inbound radio signals or transmitting only when sensor senses a critical signal.

1.4 Power Profile

As the in case of the transmitter all the power consuming blocks in the microsensor can be duty cycled for longer supply life and better operational integrity, fig 1.4. The passive sensors especially can remain all the time as they don't consume power. Processors on the other had can turn on periodically or when triggered by a sensing event. The processor evaluates the data and turns on the transceiver only when there is an event to communicate. [30] presents an algorithm for power profile optimization of microsensors to have minimum on-board energy storage. Here the battery voltage provides a measure of the energy in the system and the only when battery reaches the sense voltage it has enough energy to sense the events. The microsensor will continuously sense vents and transmit when the battery voltage reaches the transmitting threshold. Even when battery is not being charged the battery should be sized such that it has enough energy to send power down information to the base station. This way the power profile not only depends on the demand of transfer but also on the energy level of the system. Typically the energy in flow should compensate for the losses as well as the power consumption of the sensor to guarantee perpetual supply lifetime of the sensor.

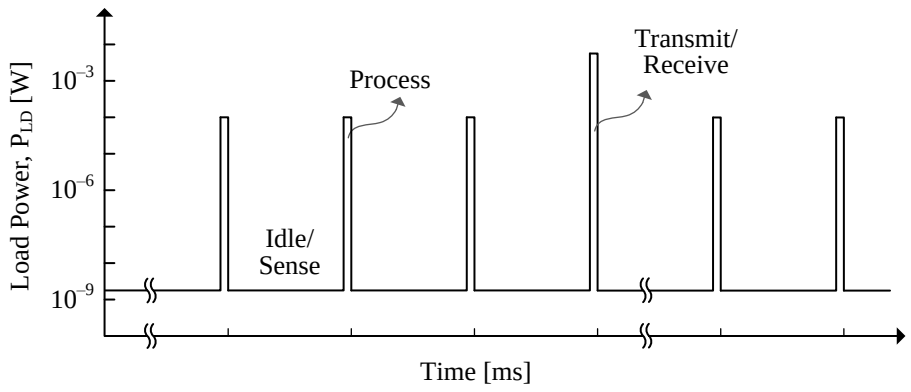


Fig. 1.4. Power profile of wireless sensor node.

1.5 Lifetime

The lifetime of the sensor typically refers to the operational life of the system. The on-board energy storage, recharging ability, physical or electrical deterioration of the components are few factors that determine the operational life of the sensor. For example, a 2x2x1 mm^3 thin film Li-ion battery [31] can supply a 100 µW power consuming sensor load only for 10 days. The sensors that have recharging capability can however extend the lifetime of the sensor perpetually. . Typically the energy in flow should compensate for the losses as well as the power consumption of the sensor to guarantee perpetual supply lifetime of the sensor. Another aspect is the deterioration the parts in the system, the CMOS and MEMS circuits can functional for more than 30yrs, but eventually electron migration in the traces can weigh down the performance. The lifetime of the sensor is determined by the block that has least lifetime, especially batteries can charge and discharge while maintaining energy capacity only for few thousand cycles, but shallow charging and discharging can extend the lifetime. Overall selection of energy sources eventually determine the lifetime of the sensor.

1.6 Sources

The sources can be classified into two major categories energy sources and power sources. Power sources have limited energy capacity however can supply a large amount of power. Power sources are typically batteries for example capacitors, inductors, electrochemical cells and super capacitors. Energy sources on the other hand have an optimal power level for optimum operation but can indefinitely supply energy. Energy sources are typically energy harvesters that harvest energy from the environment, fuel cells and atomic cells. The ragone plot [32]–[35] in Fig. 1.5 shows the plot of energy density and power densities.

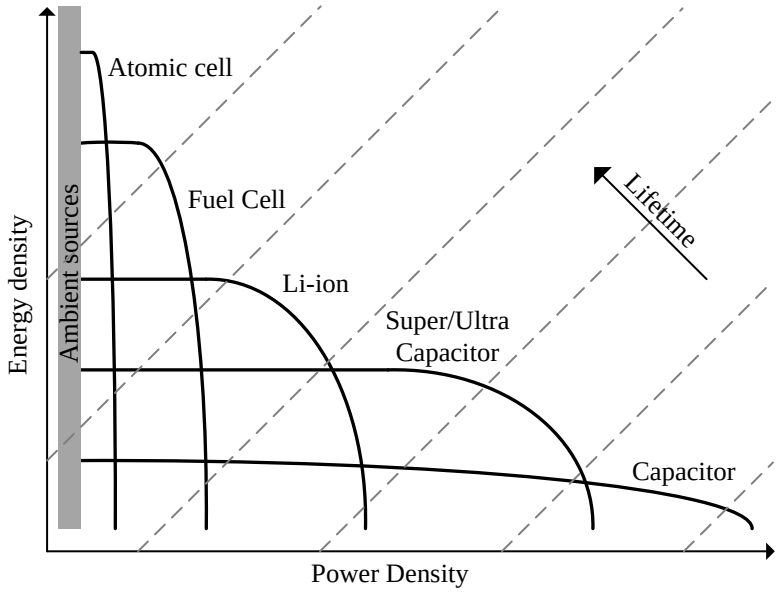


Fig. 1.5. Ragone plot of typical power and energy sources.

Ideally for a battery the energy versus power should be flat line, however in Fig. 1.5 it curves because at higher power levels the ESR of the source incurs sufficient losses to burn the stored energy, so at higher power levels it can only supply limited energy. Conversely for energy source especially harvesters the energy can be infinite at low

power levels as the harvesters can consistently harvest energy from the environment, however they have limit on the maximum power point beyond which the harvesters discharge instantly.

1.6.1 Power Sources

Power sources have limited energy capacity however can supply a large amount of power. Power sources are typically batteries [36]–[37] for example capacitors, inductors, electrochemical cells and super capacitors. Table 1.2 shows the energy density of the power sources.

Table 1.2 Energy densities of power sources

Technology	Energy density (Wh/Kg)	Cycle life	Rated voltage (V)
NiCd	45–80	1500	1.2
NiMH	60–120	300–500	1.2
Li-ion	110-160	500–1000	3.6
Thin-film Li-ion	100-130	300–500	3.6
Super-capacitor	0.5–15	10^4–10^6	2.5

1.6.1.1 Capacitors

The capacitors typically have two parallel metal plates with dielectric in between them. The parallel plates have equal and opposite charge on them to store energy. If a potential difference is imposed across the dielectric it generates an electric field which causes positive charge to accumulate on one side and negative charge to accumulate on the other side. For the capacitance value C_{CAP} and voltage V_C the energy that the capacitor store is $0.5C_{CAP}V_C^2$. There are different kinds of capacitor based on the type of material used, for example, electrolytic, ceramic and tantalum capacitor. Ceramic capacitors have the

lowest ESR therefore can supply the maximum power, however their capacitance change with temperature voltage and aging effects. However the certain ceramic capacitance has low voltage and temperature coefficients. Electrolytic capacitors can provide high value of capacitors. Tantalum capacitors have the stable capacitors among the lot. In the wireless microsensors the low ESR ceramic capacitors can provide bypass capacitance in parallel with input sources, output loads and batteries. The typical energy density of ceramic capacitors is 45 $\mu J/mm^3$.

1.6.1.2 Inductors

The inductor typically consists of a wire wound around a core. Energy is stored in the magnetic field as long as current flows through the wire. The time varying a magnetic field induces a voltage which resists the change of current flowing. The energy in the inductor with inductance L_X with current i_L flowing through it stores energy $0.5L_X i_L^2$. The limitation of inductor as storage is the ohmic power lost in the inductor ESR as the current needs to keep flowing to store energy. However the inductor serves to transfer energy between different voltage sources and loads efficiently.

1.6.1.3 Electrochemical cells

The electrochemical cells convert chemical energy to electrical energy by chemical reaction that transfers electrons from anode to cathode across an electrolyte [36]–[37]. There are various battery technologies depending on the chemical composition for example nickel cadmium (NiCd), nickel metal hydride (NiMH) and Lithium-ion (Li-ion). The nickel based technologies have lower energy densities than Li-ion and suffer from higher discharge rates and memory effects, they operate around a typical voltage of 1.2

V. NiCd have toxic Cd therefore they need to be properly disposed of. The Li-ion battery has the highest power and energy density among the cells, lower discharge rates and less memory effect and doesn't need to be frequently charged. The Li-ion technology also lends itself to thin film fabrication that helps in miniaturization and in package integration. The Li-ion batteries have optimal charging profile with constant trickle pre-charging, constant high current in between charging and constant voltage charging to complete the charging. Li-ion batteries can damage if stored long time without charge and are relatively expensive.

1.6.1.4 Super Capacitors

The electrical double-layer popularly known as super/ultra-capacitor provides the twin advantage of energy density and fast response. As such their performance fits between the battery and electrostatic capacitors [39]. Super capacitor has a liquid electrolyte dielectric between metallic electrodes and this differentiates it from standard electrostatic capacitor. The liquid electrolyte allows for a much closer parallel plate capacitor and thus provides higher capacitance per unit area. The energy density of standard super capacitor is around 0.5 Wh/Kg as table 1.2 shows. The typical super capacitor employs carbon electrodes with a permeable film that allows contact with the electrolyte. The area and volume of the carbon electrodes defines the capacitance. The break down voltage of electrolyte sets the super capacitors breakdown rating and limits the energy storage capacity. Additionally these capacitors in comparison to battery cells have lower ESR's and therefore can provide higher peak currents at lower losses. The super capacitor can charge and discharge about 10^4 to 10^6 cycles before the capacity deteriorates. Another advantage is the simple charge and discharge profiles compared to Li-ion batteries, but

they have larger self-discharge rates. The operational voltage of the capacitor spans over a larger ranges than of the batteries.

1.6.2 Energy Sources

Energy sources on the other hand have an optimal power level for optimum operation but can indefinitely supply energy. Energy sources are typically energy harvesters that harvest energy from the environment, fuel cells and atomic cells. Table .13 shows the power density of energy sources [39]–[52].

Table 1.3. Power densities from energy sources

Sources		**Transduction Mechanism**	**Estimated Power Density**
Light	Solar	Photovoltaic(PV)	< 15 mW/cm^2
	Indirect		10–100 µW/cm^2
Motion		Electrostatic	50–100 µW/cm^3
		Electromagnetic	< 1 µW/cm^3
		Piezoelectric	50–300 µW/cm^3
ΔTemp. (10 ^{O}C)		Seebeck	5–15 µW/cm^3

1.6.2.1 Ambient Sources

The environment provides various sources of energy in the form of light, motion, temperature gradient, electromagnetic waves that tiny transducers can harvest to continually supply energy, and thereby extend the energy lifetime of the sensor indefinitely. As shown in Fig. 1.5 the energy harvests can supply infinite energy when the load is less than the maximum power the source can produce.

1.6.2.1.1 Motion

The motion or vibration is an abundant source in the environment for example, moving parts in machine, air-ducts and human body. The transductions methods that enable the conversion of mechanical energy to electrical energy are electrostatic, piezoelectric and electromagnetic.

In electrostatic transducers the distance between the electrodes of a charged capacitor changes due the vibration changing the capacitance. The mechanical motion works against the electrostatic force between the parallel plates of the capacitance thereby storing energy in the capacitor. In another method the mechanical force stretches or compresses the dielectric changing the dielectric constant and therefore the capacitance. The two options to extract the energy away from the capacitor are to extract charge while maintaining the voltage constant or changing the voltage while the charge remains constant. The harvesting circuit in this case needs to invest energy to the capacitor at the beginning of the cycle and extract the energy away from the capacitor before the end of the cycle. The MEMS fabrication allows for microfabrication of the capacitor in a SiP system.

Piezoelectric transducer converts energy from mechanical stress to electric charge by the piezoelectric effect. In the absence of strain piezo electric materials are electrically neutral, application of mechanical force changes the alignments of charge centers away from each other generating the voltage. The voltage across the material changes with the strain generating an AC voltage for a periodic oscillation. The typical transducer implementation includes a miniature cantilever load with mass at the end and

piezoelectric material layout on top of the cantilever that strains as the vibration move the cantilever up and down. Since the voltage is AC to charge the battery the power transfer circuit needs an AC/DC circuit.

In electromagnetic transducer the relative motion of a magnet with respect to a coil induces the electromotive force across the coil and can supply a load connected across it. However this technique needs a magnet that is not easily fabricated with MEMS and CMOS fabrication and hence expensive.

The motion based transducers harvest maximum energy when the mechanical structure resonates. Vibration based harvester outputs energy proportional to the oscillation frequency however the naturally occurring vibrations are generally in the rang of few hertz to hundred hertz. Therefore the power densities are only between 50 – 300 μW.

1.6.2.1.2 Heat

The thermal energy sources available in the environment are human body, processors with heat sink. The transduction mechanism that converts heats to electrical energy is Seebeck effect. The transducer consists of multiple thermopiles that connect in series or parallel to supply energy. The hot end of semiconductor generates more charge carrier than the cold end, the excess carrier concentration diffuses away from the hot end towards the cold end. Therefore P type materials generate excess holes and N-type materials generate excess electrons. Shorting the hot end electrically and thermally and cold end just thermal allows for a flow of current which when drops across a load generates voltage completing the conversion. MEMS techniques can fabricate the

thermopiles from silicon and so are inexpensive and integrates well. However miniature size transducer rarely allows for large temperature difference therefore the power levels are quite low in few microwatts.

1.6.2.1.3 Light

In a semiconductor material with a P-N junction, the electron and hole concentration difference between the P-type and the N-type regions cause the electron and holes to diffuse across the junction. The carrier diffusion leaves behind immobile ionized parent atoms constituting the depletion region, exaggerated in Fig. 2.1a. The immobile ions in the depletion region establish a built-in electric field ε_{PN} that opposes the carrier diffusion, resulting in no net current flow. However, when light falls on the semiconductor material, it excites the loosely bound outer shell (valence) electrons to break away from their home site to generate electron hole pairs (EHPs) [53]–[59]. The material absorbs photons in the light as it passes through; as a result, the concentration of EHPs decreases with depth in Fig 2.1b. Interestingly, higher-energy lower-wavelength photon generates more EHPs near the surface [55].

The EHPs that breaks free from their home sites diffuse in the all the directions and recombine unless they reach the depletion region, where ε_{PN} can separate them. Most of the EHPs in, and within a hole diffusion length L_H and electron diffusion length L_E from the depletion region have high chance of separating. The result is that ε_{PN} carries electrons that reach the depletion region to the N-type side and holes to the P-type side, as Fig. 2.1a shows. This carrier flow establishes a photonic current i_{PH} whose current density J_{PH} rises with L_E, L_H, and depletion width W_D. Higher donor and acceptor doping concentrations in the N- and P-type regions increase the chance of EHPs recombining and shorten L_E and L_H. Metallic contacts shield the light from reaching the

semiconductor, therefore, reducing J_{PH}. Irregularities in surface can also trap charges to reduce the photonic current.

1.6.2.2 Alternate Sources

Other sources that provide energy are fuels cells and atomic cells.

1.6.2.2.1 Fuel cells

Fuels cells coverts the energy of a chemical reaction to electrical energy [60]–[65]. They typically produce non-toxic clean by products. In a fuel cell the catalyst at the anode oxidize the fuel that passes through it to generate positive hydrogen ions, protons and electrons. These pass through the electrolyte and the electrons flow out into the external circuit to generate power. The hydrogen protons continue through the electrolyte to reach the cathode where it oxidizes in presence of oxygen and electrons. The most popular fuel is the direct methanol fuel cell (DMFC) that uses a liquid fuel [34] and thus comparatively more potable than solid fuel operating cells. The power that fuels cells can provide are typically low at around 50–100 μW [35]. However the minimum size centimeter fuels cells are large in reference to the wireless micro sensor applications. Additionally the need to refuel and the deterioration of the electrolyte membrane over longer application times can lead to prohibitively large replacement costs.

1.6.2.2.2 Atomic cells

Operation of betavoltaic atomic [66] cells is similar to photovoltaic cells except here the beta particles replace the photons. The high-energy beta particles can generate many electron-hole particles, however much of the energy is lost as phonons. However flux of

beta particles is much smaller than light therefore the power levels are lower around 10s of microwatts. Disadvantage of atomics cells are high cost, safety issues with radioactive materials and availability [32].

1.7 Power-Assisted Energy Sources

Photovoltaic (PV) cells, for example, can generate 15-mW/cm^2 from solar light, which is orders of magnitude higher than what piezoelectric, electrostatic, electromagnetic, and thermoelectric generators can from motion, radiation, and heat [39]–[52]. Unfortunately, sunlight is not always available, and indoor lighting is a poor substitute. Plus, millimeter cells only capture a small fraction of the incoming light. So the only way the intermittent microwatts that small PV cells generate can sustain a wireless transmitter, for example, which draws milliwatts at a time, is with assistance from an on-board battery like Fig. 1.6 shows.

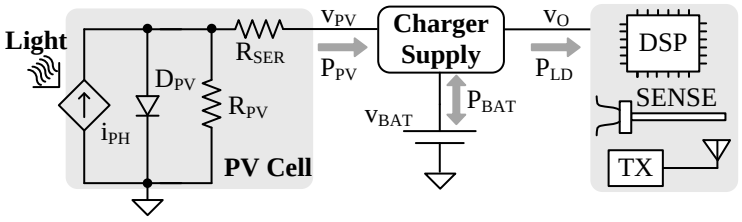


Fig. 1.6. Battery-assisted photovoltaic-harvesting microsystem

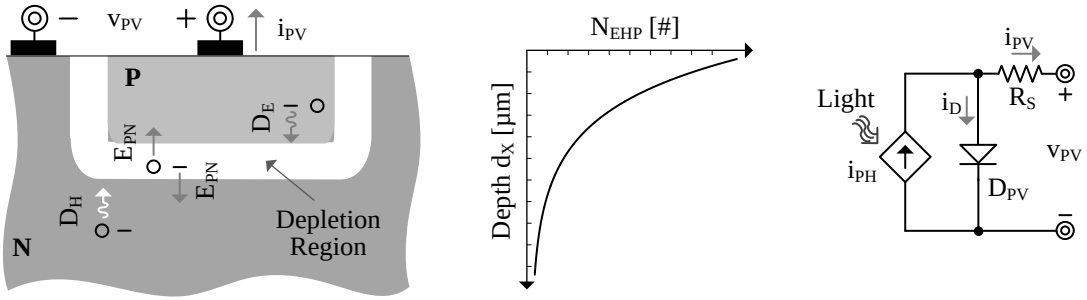
Since small sensors can idle between sensing and transmission events, they can, between these times, consume nanowatts of the microwatts that PV cells supply. A wireless microsystem can therefore replenish its battery v_{BAT} with excess PV power between heavily loaded periods. So if loading events are sufficiently sparse and short term, v_{BAT} can charge long enough to help the system supply high-power loads. For

maximum functionality and life, the system should draw maximum power from the PV cell [68]. And for maximum integration, the battery should be small, so the system should require little battery assistance. The charger–supply should also deliver as much power as possible.

CHAPTER 2. PHOTOVOLTAIC CELLS

2.1 Basic Operation

A PV cell is essentially a P–N junction, so immersing N- into P- or P- into N-type semiconductor regions like Fig. 2.1a illustrates is the basic recipe for building cells. The sharp charge-carrier concentration gradients across the junction cause electrons and holes to migrate into the opposing regions. This diffusion process depletes parent atoms near the junction of charge carriers. The immobile atoms therefore ionize and impose a built-in electric field E_{PN} across the depletion region. In steady state, E_{PN} induces a drift current that is equal and opposite to the diffusion current that produced E_{PN} in the first place. As a result, net current flow is zero.



(a) (b) (c)

Fig. 2.1 PV P–N junction (a) profile, (b) carrier concentration, and (c) model.

When light passes through the semiconductor material, high-energy photons excite loosely bound electrons with sufficient energy to break them away from their home sites. Under the influence of E_{PN}, liberated electron–hole pairs (EHPs) in the depletion region separate and drift in opposite directions: holes to the P side and electrons

to the N side. The net result is the photonic current i_{PH} shown in Fig. 2.1c. Because wider depletion regions collect more EHPs, higher depletion widths W_D raise i_{PH}.

Minority electrons liberated in the P side and minority holes liberated in the N side diffuse, on average, one diffusion-length L_E or L_H before recombining with majority carriers. This means, a fraction of EHPs liberated within L_E and L_H of the depletion boundaries of the junction reach the depletion space to add to i_{PH}. Farther-away EHPs recombine, so they do not contribute to i_{PH}. In other words, longer diffusion lengths L_E and L_H aid the generation process.

$$J_{PH} \propto L_E + L_H + W_D \tag{2.1}$$

Because the material absorbs light energy, light intensity is greatest near the exposed surface. Photons therefore liberate more EHPs near the surface than deeper in the material. In fact, EHP concentration N_{EHP} falls exponentially with depth, as Fig. 2.1.b shows. And when wavelengths are short, light does not penetrate the material as far, so N_{EHP} is higher near the surface and penetration depth is shallower [53].

$$N_{EHP} = N_S e^{-A_\lambda d_S}. \tag{2.2}$$

All this means, depletion regions near the surface collect and generate more i_{PH}, especially when wavelengths are short.

2.2 Loss Mechanism

Liberating EHPs is how P–N junctions convert light energy into the electrical domain, and collecting and steering them to the load is how they output power. The first loss in

this process is the fraction of light energy lost to heat. Blocked and reflected light, ohmic power, uncollected EHPs, and collected EHPs lost are other losses. This is why conversion efficiency, which is the fraction of input light power that reaches the load, is normally low at 10%–40% [53]–[59], [67].

2.2.1 Shading and Reflection

Standard photovoltaic technologies diffuse and implant dopants into a silicon substrate to define N- and P-type regions and deposit metal layers above the regions to interconnect them. Unfortunately, these same metal layers shield a cell from incoming light, so the exposed window is smaller than the actual cell. Blocked light is therefore a loss. Surface of the photovoltaic cells have protective coating to prevent reaction to the environment gases. In case of silicon substrates SiO_2 and SiN_X though mostly transparent the layers reflect light. The silicon surface reflects about 30% of the useful incident light and causes loss.

2.2.2 Ohmic Loss

The semiconductor and metallic links that connect the edges of the depletion region to the load impose series resistance R_S to PV current i_{PV}. So when i_{PV} flows, R_S burns power. Although adding metal and raising doping concentrations reduce resistance, more metal blocks light and more majority carriers shorten diffusion length. This means, ohmic losses fall as shading losses and uncollected EHPs rise. Since photovoltaic power P_{PV} increases linearly with i_{PV} and ohmic loss with i_{PV}^2 the ohmic losses are a dominant fraction at higher P_{PV}.

2.2.3 Uncollected EHPs

Some of the EHPs that light generate recombine before E_{PN} separates them to constitute recombination losses. The major mechanisms of recombination are Shockley-Read-Hall (SRH), auger, radioactive and surface recombination [53].

Liberated minority carriers that recombine with majority carriers constitute a loss to photonic current i_{PH}. Because higher doping concentrations raise the number of majority carriers with which minority carriers can recombine, EHPs in highly doped regions diffuse less. And with shorter diffusion lengths, less number of EHPs reaches the depletion region. So, higher donor and acceptor doping concentrations, N_D and N_A, in the N- and P-type regions generate less i_{PH}.

Irregularities on the surface can also trap liberated EHPs long enough for EHPs to recombine [53]. Filling the gaps with dopant atoms can reduce this loss, but not without supplying majority carriers near the surface. So, heavily doped surfaces help only when the loss to traps is more severe than the loss to majority carriers near the surface.

2.2.4 Diode Leakage

As just described, PV output current i_{PV} in Figs. 2.1a and 2.1c flows out of the cell and into a load, so the voltage across the load and the cell v_{PV} is positive. This means, the P–N junction that generates i_{PH} forward-biases, and the diode D_{PV} in the junction steers a fraction of i_{PH} away from the load to ground. Leaked power climbs with higher doping concentrations N_A and N_D because they strengthen the diode.

2.3 Maximum Photovoltaic Power

For a given light, photonic current i_{PH} delivers more power P_{PH} when the voltage across the cell v_{PV} is higher. Unfortunately, the same is true for the power lost in the diode P_D. But since P_{PH} rises linearly and P_D rises exponentially with v_{PV}, gains first outpace losses when a low v_{PV} rises and losses then outpace gains when a high v_{PV} rises. So like Fig. 2.2 shows, output power P_{PV} rises with v_{PV} when v_{PV} is low and falls when v_{PV} is high. The maximum power point (MPP) $P_{PV(MPP)}$ results when the rise in losses cancels the rise in gains, at the optimum PV voltage $v_{PV(OPT)}$ for that particular light setting.

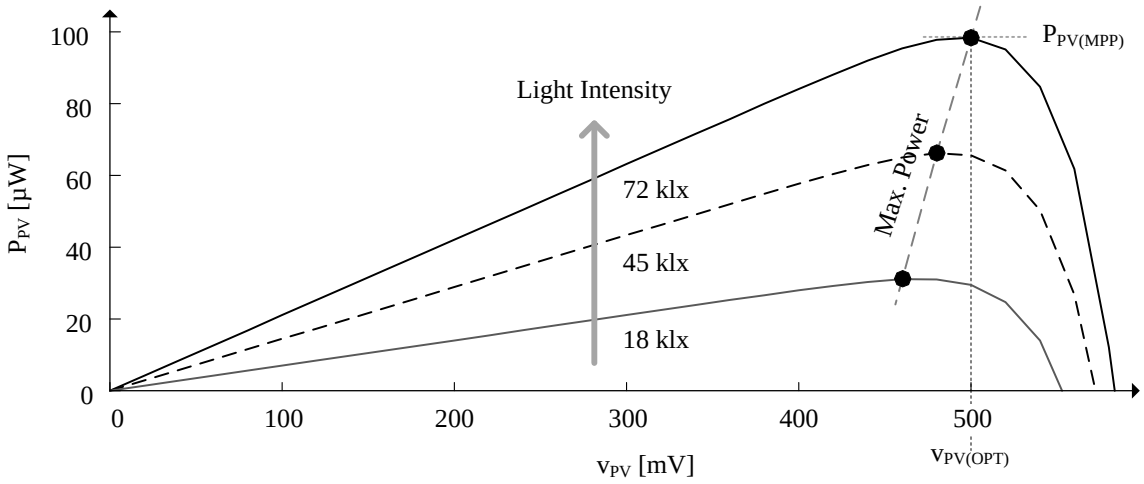


Fig. 2.2 Measured PV power across PV voltage for several light levels.

To harvest maximum power from the PV cell the system needs to track the maximum power point [68]. The two important aspects of maximum power point tracking (MPPT) is one sensing the photovoltaic power or equivalent and then identifying or tracking its maximum value to operate the system about that point.

2.3.1 Sensing

The first aspect of tracking is sensing the quantity to track. From the photovoltaic cell point of view the straight forward method of sensing photovoltaic power is to measure v_{PV} and i_{PV} separately and multiply them to generate P_{PV} [68]. However the multiple measurements and multiplication can be taxing to micro power systems. Fortunately to track maximum power point it is not necessary to make accurate measurements of the absolute power values, instead sensing quantities that vary proportionally with P_{PV} is sufficient. The short circuit current i_{SH} and open circuit voltage v_{OC} of the PV cell are two such quantities that are representative of P_{PV}.

As discussed in the previous subsection PV cell can essentially be modelled as photonic current i_{PH} in parallel with diode, here i_{PH} is directly proportional to photon intensity and therefore P_{PV}. By short circuiting the PV cell i_{PH} can be sensed. Similarly in the open circuit condition the i_{PH} completely flows into the diode this way since diode characteristics do not change appreciably with light level the diode voltage in open circuit conditions varies proportionally with i_{PH} and P_{PV}.

Another way to indirectly sense the P_{PV} is measuring parameters of circuits that draw power from it. In a photovoltaic-charger the charger circuit extracts power from PV cell to charge the battery. Here the battery power P_{BAT} is proportional to P_{PV} and since battery voltage v_{BAT} is constant or varies slowly, battery charging current i_{BAT} is proportional to P_{PV}. The voltage across a series resistor and a sensing MOSFET to mirror a fraction of battery current are popular methods to sense current [69]. In charger circuits

operating in discontinuous mode, the on duration of the battery switch can also be a measure of P_{BAT} [70].

2.3.2 Tracking

The profile of the photovoltaic current and parameters proportional to it resemble a hill with a peak at an optimum photovoltaic voltage $v_{PV(OPT)}$. To track the maximum power point at given light condition the tracking circuits varies the voltage across the PV cell and look at variation in power and continues to do it until peak value is reached. The most prominent methods to track MPPT are the hill climbing and fractional parameter methods

2.3.2.1 Hill Climbing Technique

2.3.2.1.1 Fixed Step Size

In the fixed step size hill climbing algorithm also known as perturb and observe method [71]–[75], the tracking circuit changes v_{PV} with fixed increments Δv_{PV}. If ΔP_{PV}, the change in P_{PV} with Δv_{PV}, is greater than zero or positive continue incrementing v_{PV}. Similarly, if ΔP_{PV} is smaller than zero reduce v_{PV}. In other words increment or decrement v_{PV} so as to increase ΔP_{PV}. It is important to note here that absolute value of P_{PV} is not important but only the change in P_{PV} matters.

In Fig 2.3 as v_{PV} increases P_{PV} increases from P_{PV1} to P_{PV10} in multiple increments of v_{PV}. As v_{PV} increases further P_{PV} falls indicating the crossing over of the peak value. To complete tracking the v_{PV} can decrement once to set the MPP at $P_{PV10.}$ In this method the as the step sizes are quantized there could be error P_{ERR} between the actual MPPT value

and the identified one. One solution is to reduce the step size so that P_{ERR} is low, however smaller step size lead to longer tracking time and therefore longer duration away from drawing maximum power.

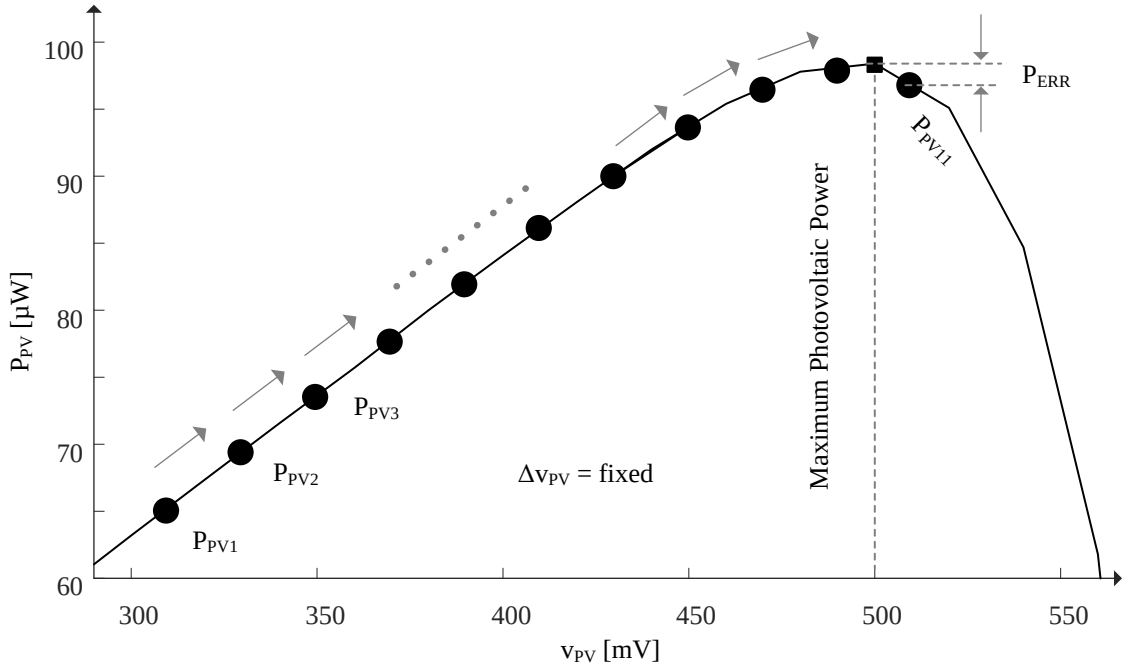


Fig. 2.3 Hill climbing algorithm.

2.3.2.1.2 Variable Step Size

One solution to reduce P_{ERR} without compromising on tracking speed is to vary the step size [76]–[81] depending on location of the current operating point on the hill, Fig. 2.4. Ideally step size should be large when v_{PV} is away from $v_{PV(OPT)}$ and small when is it is around $v_{PV(OPT)}$. One way to implement this to adjust Δv_{PV} with the slope of the hill:

$$\Delta v_{PV} \propto \text{slope} = \frac{\Delta P_{PV}}{\Delta v_{PV}} \tag{2.3}$$

Near the peak of the hill P_{PV} flattens and therefore the slope and by extension Δv_{PV} is very small, and similarly away from the peak slope and Δv_{PV} are large. The draw back here is the control complexity to calculate the slope.

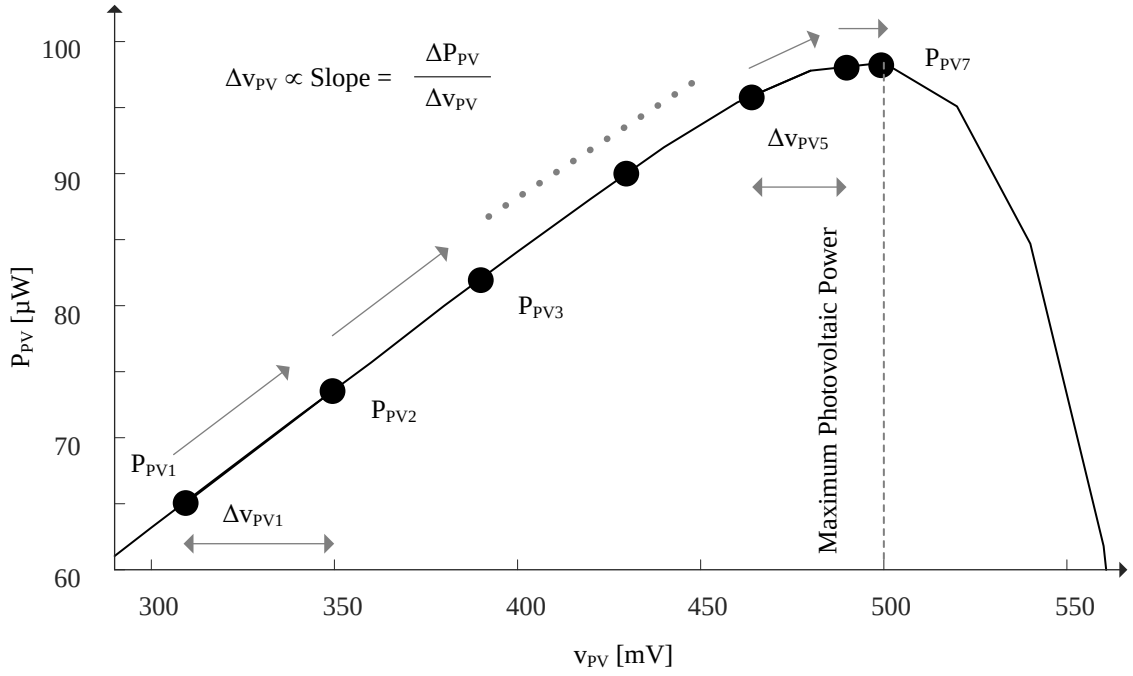


Fig. 2.4 Gradient adjusted hill climbing algorithm.

2.3.2.1.3 3-point Parabolic Technique

Another method to climb track the peak is the 3-point technique [82], Fig. 2.5. In this method each step consists of making 3 consecutive measurements that are Δv_{PV} apart. There is distinct characteristics to the relative values of P_{PV} , in Fig. 2.5, at the 3 points based on the location:

$$\begin{aligned} v_{PV1-3} < v_{PV(OPT)} &\Rightarrow P_{PV1} < P_{PV2} < P_{PV3} \\ v_{PV1-3} > v_{PV(OPT)} &\Rightarrow P_{PV1} > P_{PV2} > P_{PV3} \\ v_{PV2} \approx v_{PV(OPT)} &\Rightarrow P_{PV1} < P_{PV2} > P_{PV3} \end{aligned} \tag{2.4}$$

With these characteristics the tracking circuits increments v_{PV} values when $v_{PV1–3}$ is less than $v_{PV(OPT)}$ and decrease v_{PV} values when $v_{PV1–3}$ is greater than $v_{PV(OPT)}$. In the case when P_{PV2} is greater than both P_{PV1} and P_{PV2}, v_{PV2} defines the MPP. Here the Δv_{PV} between the 3 points should be small enough to reduce the P_{ERR} and should be large enough to reduce tracking duration.

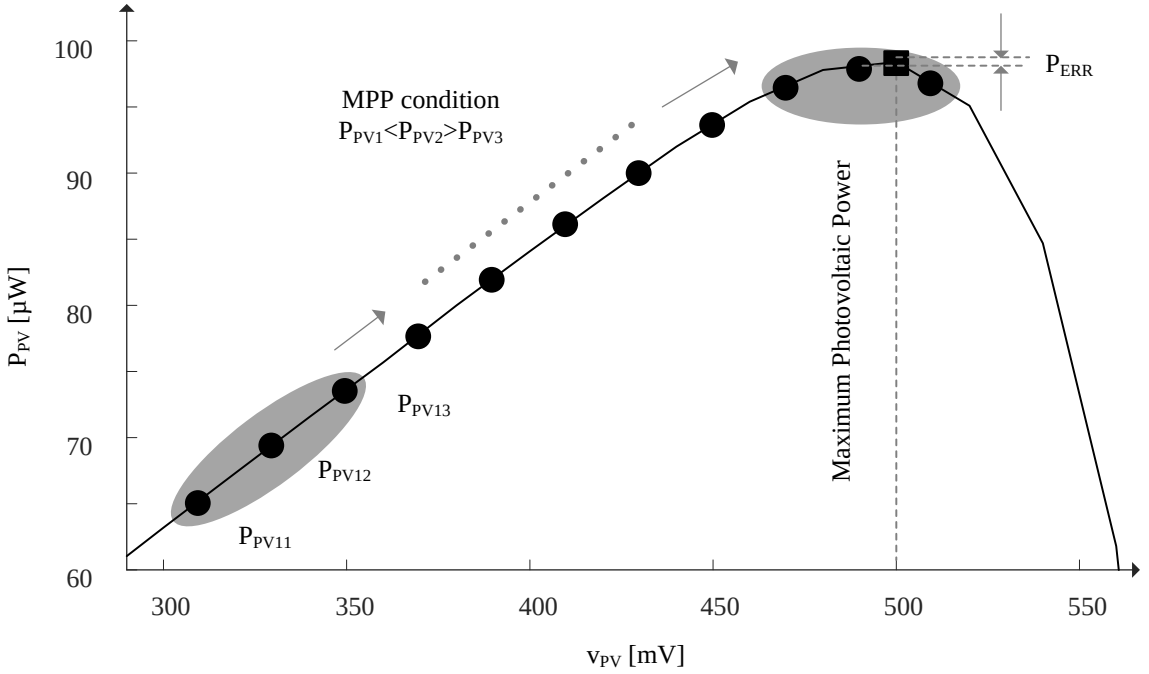


Fig. 2.5 3-point parabolic algorithm.

2.3.2.2 Fractional Parameter

As sensing section mentions the short circuit current and open circuit voltages are two parameters than uniquely represent i_{PH} and by extension $P_{PV(MPP)}$. From these values maximum power point voltage $v_{PV(OPT)}$ or current $i_{PV(OPT)}$ can be approximated as the linear translation of v_{OC} or i_{SH} [83]–[90]:

$$v_{PV(OPT)} = k_{OC} v_{OC}$$
$$i_{PV(OPT)} = k_{SH} i_{SH} \tag{2.5}$$

Here open-circuit translation coefficient k_{OC} varies between 0.71 and 0.85, and short circuit coefficient k_{SH} varies between 0.78 and 0.92 [68]. Since this method doesn't actively track power and just makes an approximation the P_{ERR} is present as shown in Fig. 2.6. Another aspect is open circuiting or short circuiting losses PV power as energy and opportunity loss. Among the methods v_{OC} is easier to implement and in circuits involves less complexity than short-circuiting PV cell, additionally k_{OC} varies less significantly than k_{SH}.

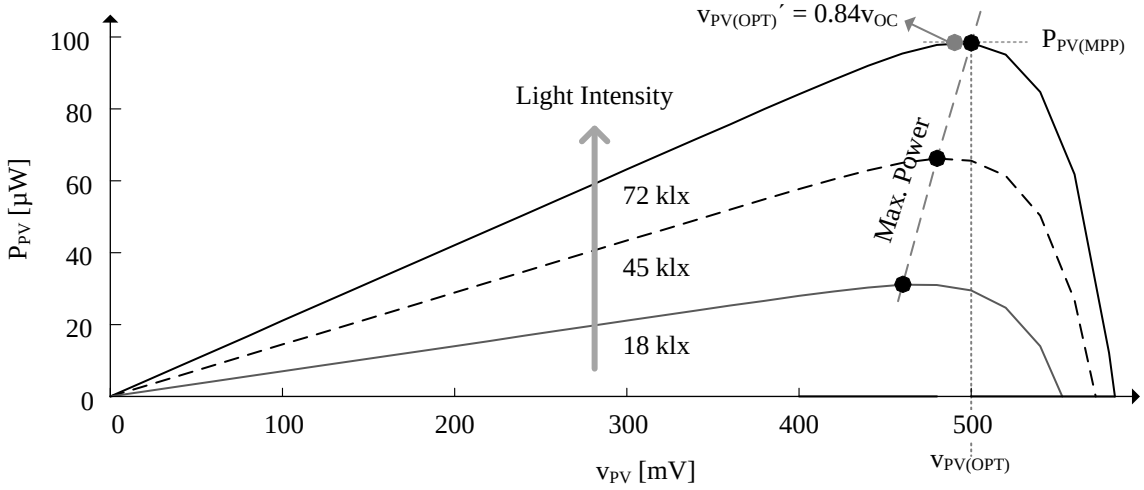


Fig. 2.6 Fractional open-circuit method.

2.4 CMOS Photovoltaic Cells

Standard low-cost CMOS technologies normally incorporate no more than shallow N^+ and P^+ diffusions for the source, drain, and bulk terminals of NFETs and PFETs and a deeper N well to isolate PFETs from the P substrate [54]–[59], [91]–[93]. Although

doping concentrations are not always the same, N^+ and P^+ have higher dopant concentrations than the well, and the well has higher concentration than the epitaxial region beneath. The epitaxial layer is deeper and usually above a heavily doped P region. So the only ways to build P–N junctions are to immerse N+ or N well into the P substrate or P+ into an N well that is in the P substrate.

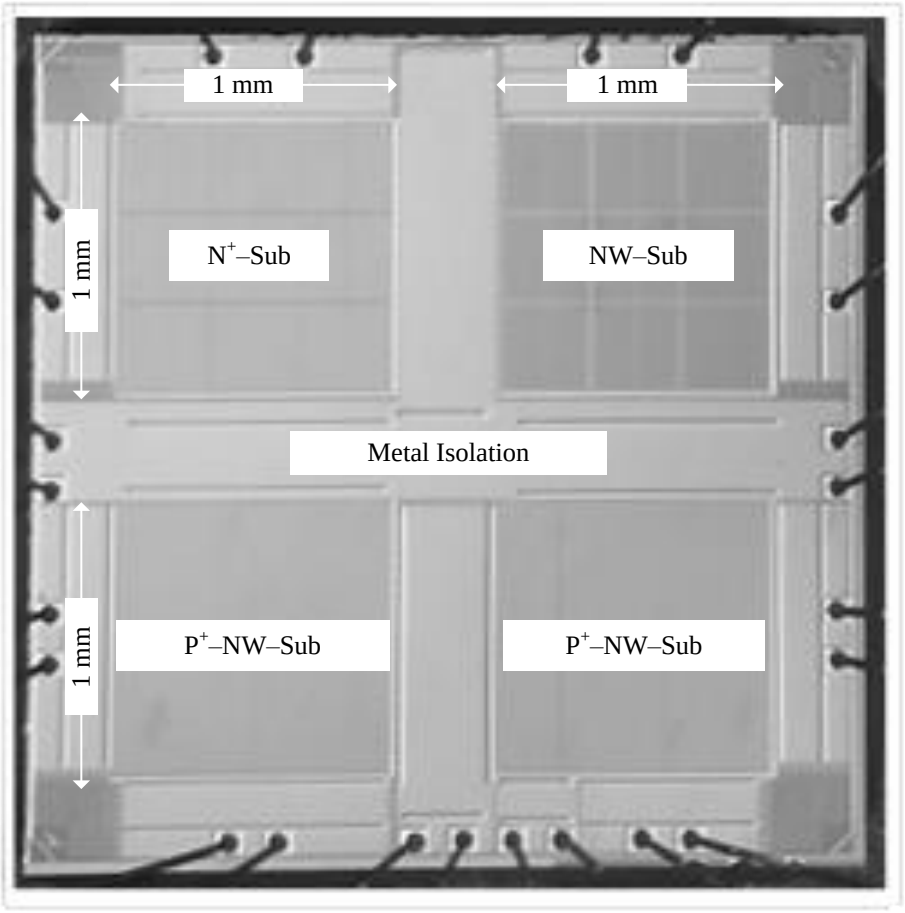


Fig. 2.7 Die photograph of the single-well CMOS PV cells fabricated.

To compare cells under equivalent constraints [59], all cells in Fig. 2.7 occupy 1 mm^2 of the same 0.35-μm single-well CMOS die, so the cost of each configuration is the same. The aim here is to design the highest power-generating configuration, and therefore comparing cells from the same technology is the most important consideration. Although

power and cost vary with pitch, relative performance changes less because pitch affects all cells in similar ways. As a result, comparing power levels and power-conversion efficiencies to others in literature is less relevant and less appropriate when doping concentrations, junction depths, and substrate thicknesses constitute proprietary information that is often unavailable.

2.4.1 N^+ in P Substrate PV Cells

Immersing N^+ into the P substrate like Fig. 2.8 shows creates a charge-collecting P–N junction. Since the doping concentration of N^+ is high and dopants are near the surface, donor atoms tend to fill surface irregularities. Minority charge carriers are therefore less likely to linger long enough to recombine. Higher majority-carrier concentration, however, also means minority holes recombine with majority electrons within a relatively short diffusion length L_H. So only a fraction of holes in the N^+ region reach the depletion space beneath. And although the region is near the surface, N^+ is also shallow, so light produces few EHPs.

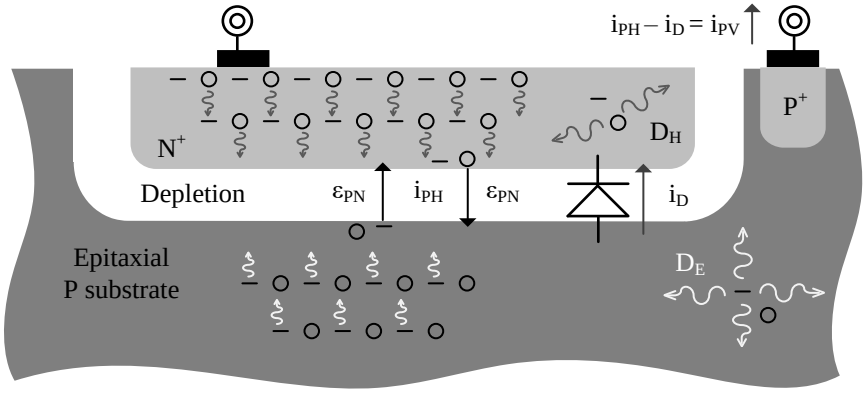


Fig. 2.8 N^+ in P substrate PV cell.

The doping concentration of the substrate is lower, so the diffusion length of

minority electrons is longer. Plus, the region is vast, which under equivalent light intensity, means more EHPs are likely to appear. But since light intensity falls exponentially with depth, EHPs are less prevalent. And since the cell can only collect EHPs within a diffusion length of the depletion space, farther-away EHPs ultimately recombine.

Measurement: When subjecting a prototyped 1-mm^2 0.35-µm CMOS structure of this sort to 1 klx, 10 klx and 80 klx, the cell generated 0.2, 1.2 and 5.9 µW, as Fig. 2.9 shows. At 80 klx, the equivalent of direct sunlight, the maximum power point was at 0.40 V and 15 µA, like Fig. 6 shows. Since photonic current i_{PH} was 16 µA (with zero volts), i_{PH} lost 1 µA to diode current i_D.

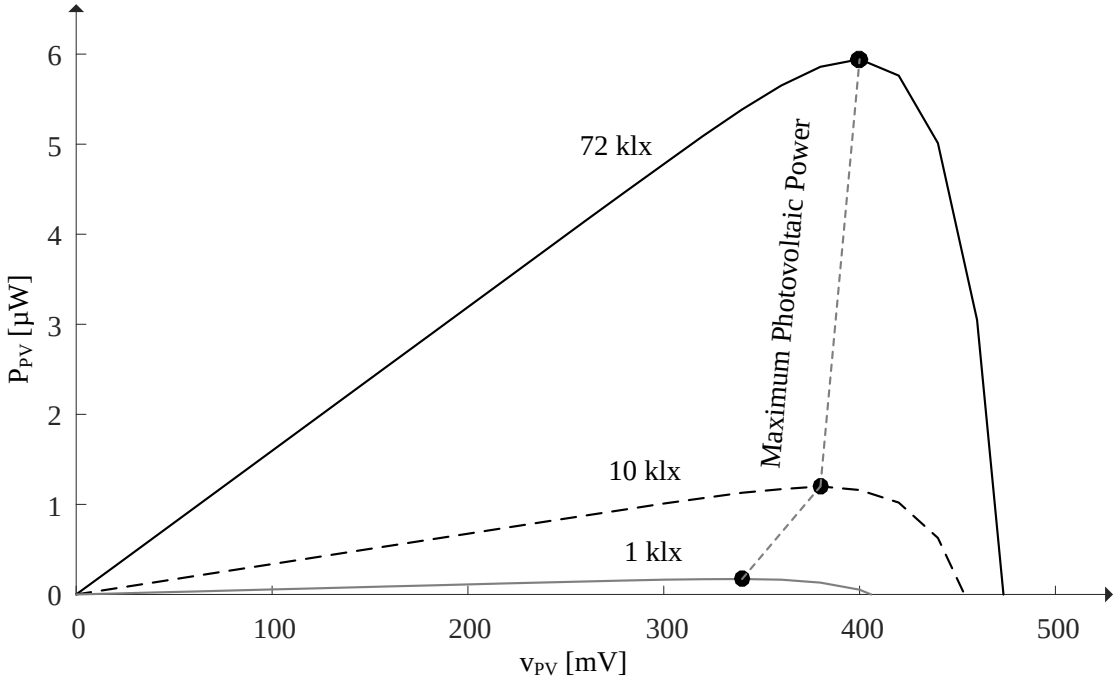


Fig. 2.9 Measured PV power across PV voltage of N^+ in P substrate PV cell.

2.4.2 N well in P Substrate PV Cells

Immersing an N well into the P substrate like Fig. 2.10 shows also creates a charge-collecting P–N junction. Since the well's doping concentration is lower than that of N^+, the average diffusion distance L_H that minority holes traverse before recombining with majority electrons is longer, so more holes can reach the depletion space beneath. Plus, lower doping concentration means the junction is easier to deplete, so the depletion space is wider and therefore capable of collecting more EHPs. The junction, however, is farther away from the exposed surface, so EHP concentration is generally lower. And like before, only substrate EHPs within a diffusion length of the junction can reach the depletion space.

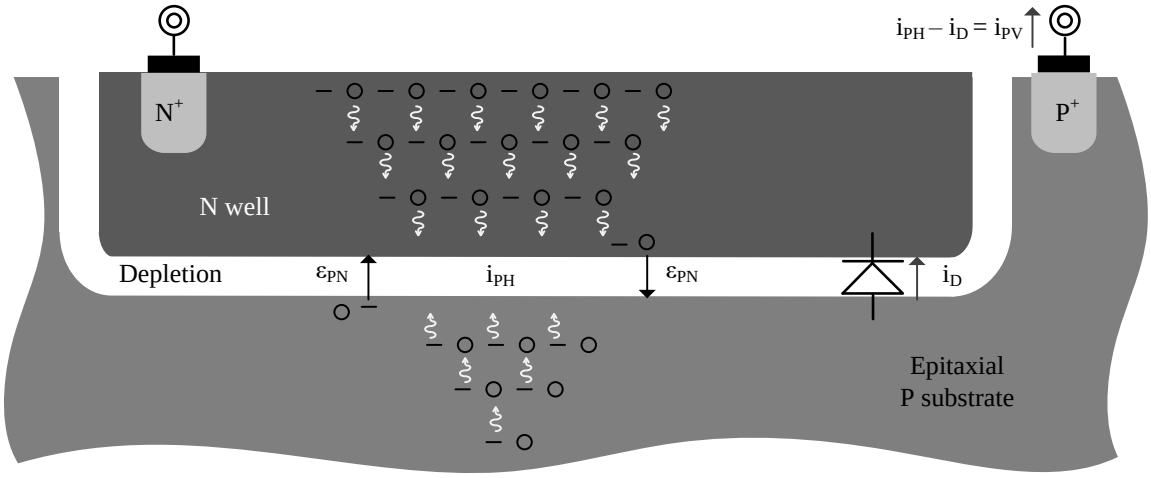


Fig. 2.10 N well in P substrate PV cell.

Measurement: When subjecting a 1-mm^2 0.35-µm CMOS structure of this sort to 1 klx, 10 klx and 80 klx, the cell generated 3.0, 20 and 98 µW, as Fig. 2.11 shows. At 80 klx, the maximum power point in Fig. 6 was at 0.50 V and 196 µA. Since photonic current i_{PH} was 210 µA (with zero volts), i_{PH} lost 14 µA to diode current i_D.

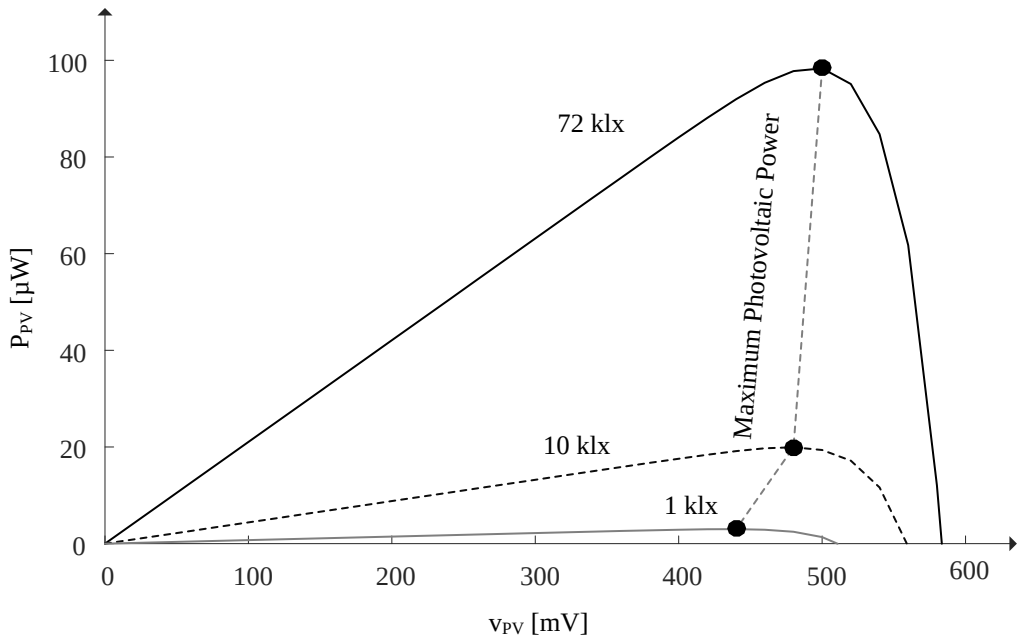


Fig. 2.11 Measured PV power across PV voltage of N well in P substrate PV cell.

2.4.3 P^+ in N Well PV Cells

Interestingly, immersing P^+ in N well in a P substrate like Fig. 2.12 illustrates creates not only two P–N junctions: P^+–well and well–substrate, but also the P^+–N well–P substrate bipolar-junction transistor (BJT). As a PV cell, nearby P^+ and N-well EHPs reach the top P^+–well junction and nearby N-well and P-substrate EHPs reach the bottom well–substrate junction. So the well contributes to the photonic currents of both junctions, to $i_{PH(T)}$ and $i_{PH(B)}$ [54]–[58].

As with N^+, the doping concentration of P^+ is high, many dopants are near the surface, and the region is shallow, so surface recombination is low, minority diffusion length L_E is short, and light produces few EHPs. Although the lower well–substrate junction is farther away from the surface, longer diffusion lengths and a wider depletion region counter the effects of lower EHP concentration. Ultimately, the performance of

this cell hinges on which photonic current the structure outputs and under what conditions.

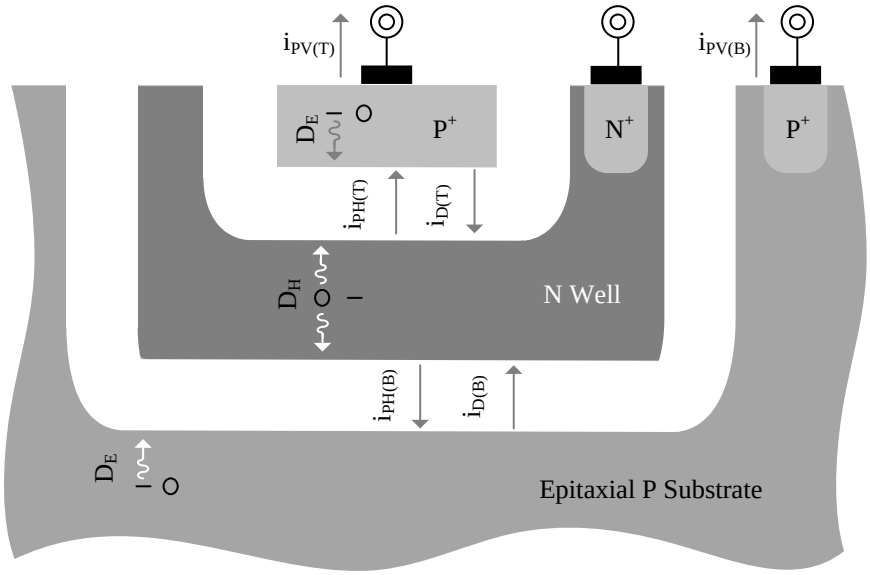


Fig. 2.12 P^+ in N well in P substrate PV cells.

2.4.3.1 Top Junction

Shorting the N well to the substrate with a metallic link steers bottom photonic current $i_{PH(B)}$ around a zero-volt loop that keeps $i_{PH(B)}$ from producing power, Fig. 2.13a. So when subjecting a standard 1-mm^2 0.35-µm CMOS structure to 1 klx, 10 klx and 80 klx, the cell generated 0.4, 3.1 and 18 µW, as Fig. 2.13b shows. At 80 klx, the maximum power point in Fig. 6 was at 0.36 V and 49 µA. Since top photonic current $i_{PH(T)}$ was 55 µA (with zero volts), $i_{PH(T)}$ lost 6 µA to top diode current $i_{D(T)}$.

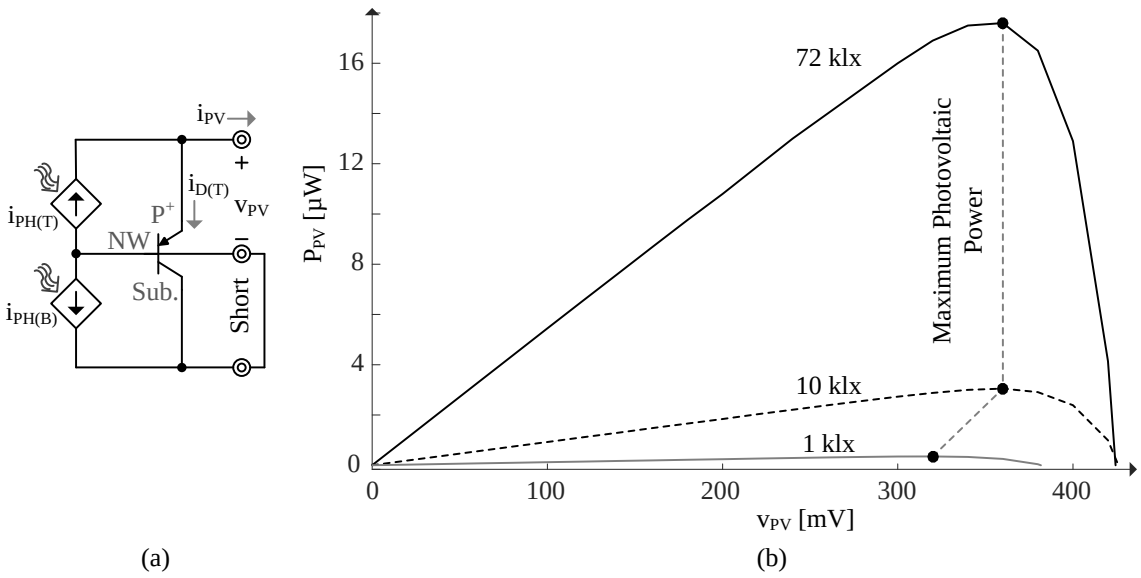


Fig. 2.13 Top junction (a) electrical model (b) measures PV power across PV voltage.

2.4.3.2 Bottom Junction

Shorting P^+ to the N well with a metallic link similarly steers top photonic current $i_{PH(T)}$ around a zero-volt loop that keeps $i_{PH(T)}$ from producing power, Fig. 2.14 a. So when subjecting a standard 1-mm^2 0.35-µm CMOS structure to 1 klx, 10 klx and 80 klx, the cell generated 3.0, 20 and 91 µW, Fig 2.14b. At 80 klx, the maximum power point in Fig. 6 was at 0.38 V and 239 µA. Since bottom photonic current $i_{PH(B)}$ was 250 µA (with zero volts), $i_{PH(B)}$ lost 11 µA to diode current $i_{D(B)}$.

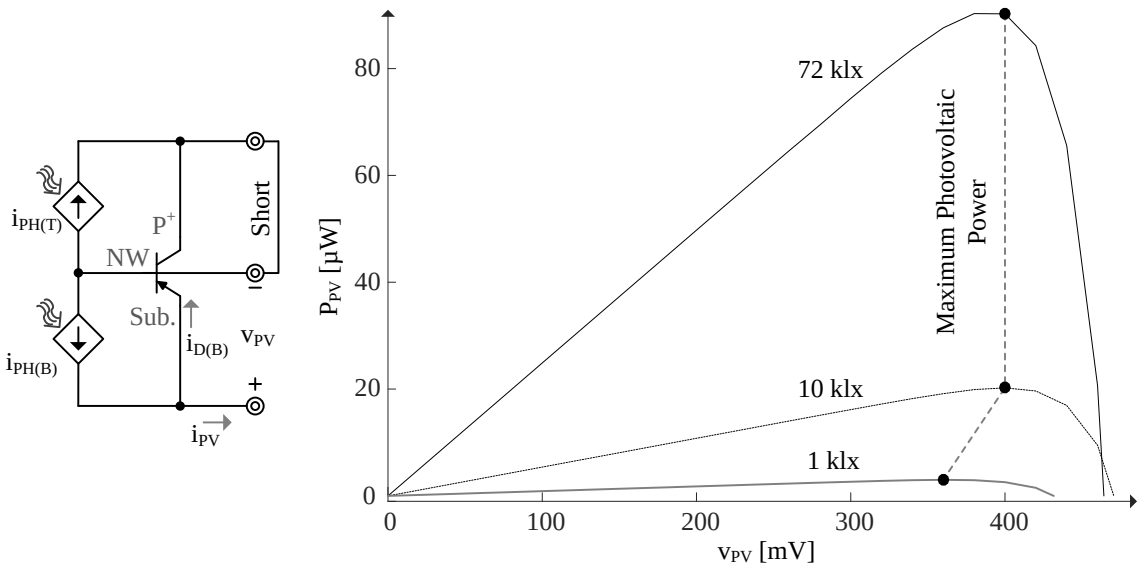


Fig. 2.14 Bottom junction (a) electrical model (b) measures PV power across PV voltage.

2.4.3.3 Combined junctions

P^+ and P Substrate Shorted: The most direct way of harvesting power from both the junctions is to short the P-type regions together with N well as the second terminal, in this scenario the BJT behaves like two diodes in parallel, as in Fig. 2.15. Both $i_{PH(T)}$ and $i_{PH(B)}$ produces power. The most of EHPs a diffusion length from either of the junctions collects to generate power-producing current. With the P type regions shorted to each other the BJT operates in deep saturation where it totally loses BJT action and behaves as two parallel diodes. The leakage for similar voltage levels in comparison to earlier P^+–NW–Sub diodes is lower. At the upper junction $i_{PH(T)}$ after losing a portion of current $i_{D(T)}$ flows out as $i_{PV(T)}$. Similarly $i_{PH(B)}$ after losing a portion of current $i_{D(B)}$ flows out as $i_{PV(B)}$.

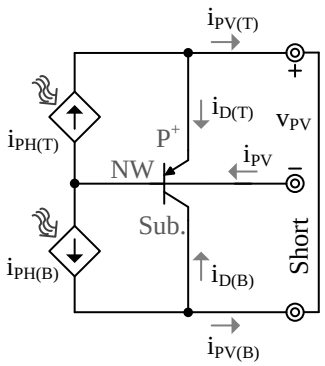


Fig. 2.15 Electrical model of P^+ and P substrate shorted.

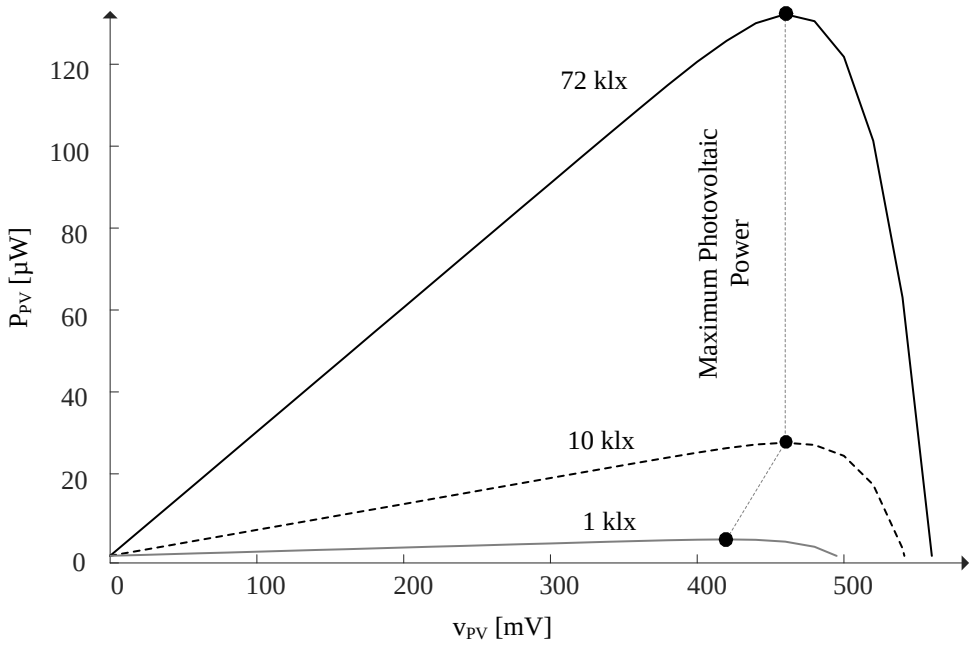


Fig. 2.16 Measurement of PV power across PV voltage of P^+ and P substrate shorted.

Measurement: The total power the photovoltaic current produces i_{PV} is the sum of $i_{PV(T)}$ and $i_{PV(B)}$. In absence of BJT action the leakages are lower and as a result, the cell produces maximum power of 4 µW, 27.6 µW and 132.2 µW, Fig. 2.16, about optimum voltages of 0.42 V, 0.46 V and 0.46 V at 1 klx, 10 klx and 80 klx. At 10 klx, $i_{PH(T)}$ and $i_{PH(B)}$ is about 9.3 µA and 54 µA, with $i_{D(T)}$ and $i_{D(B)}$ at 2.1 µA and 1 µA at $v_{PV(OPT)}$ of 0.46 V. $i_{D(T)}$ is higher than $i_{D(B)}$ as the upper junction diode is the stronger one.

At 80 klx equivalent of direct sunlight the large $i_{PV(T)}$ current drops voltage, thus P^+ is at a slightly higher voltage than P Substrate, and as a result $i_{D(B)}$ is non-existent and $i_{D(T)}$ after losing portion to base current flows out of the substrate. Here $i_{PV(B)}$ at $v_{PV(OPT)}$ is 249.2 µA slightly higher than $i_{PH(B)}$ of 247.8 µA.

Open P^+: Another option to harvest power from both junctions is to open one of the junctions, in this case the photovoltaic current at the open junction flows through the device, out through the other end, Fig.2.17. This way both $i_{PH(T)}$ and $i_{PH(B)}$ produces power. Therefore most of the EHPs a diffusion length away from either one of the junctions separates to produce current. With P Substrate held v_{PV} above the N Well, as in Fig. 6b, this cell produces power. The $i_{PH(T)}$ current flows through the BJT, biasing it with P^+ as emitter, N Well as base and Substrate as collector. When v_{PV} is low BJT is in active region as a result most of $i_{PH(T)}$ after losing a portion as base current and all of $i_{PH(B)}$ forms i_{PV}. Here P_{PV} is low as v_{PV} is low. To produce maximum P_{PV} both v_{PV}, i_{PV} has to be high and this happens when BJT is in saturation.

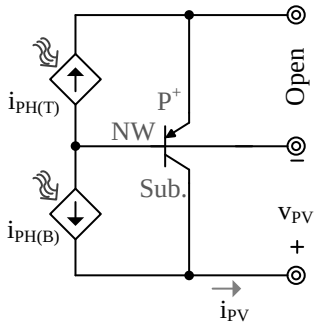


Fig. 2.17 Electrical model of P^+ open.

Measurement: The cell produces maximum power of 4 µW, 27.4 µW and 131.7 µW, Fig. 2.18, about optimum voltages of 0.42 V, 0.46 V and 0.46 V at 1 klx, 10 klx and

80 klx. At 80 klx equivalent of direct sunlight, i_{PV} is around 286 µA at $v_{PV(OPT)}$ of 0.46 V.

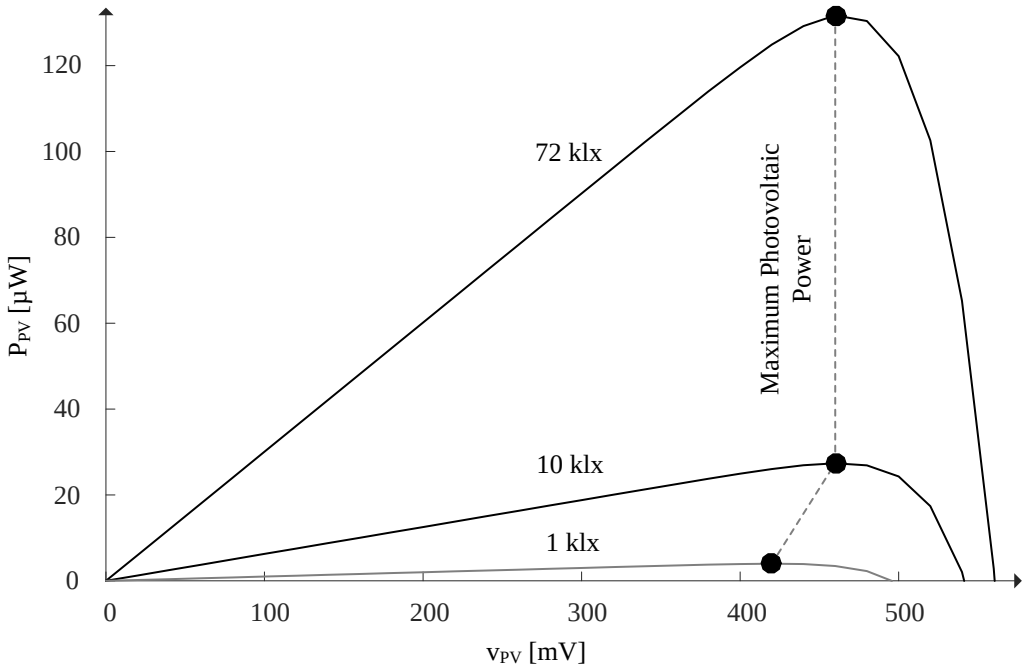


Fig. 2.18 Measurement of PV power across PV voltage of P^+ open.

Open P Substrate: Similar to the earlier case when P substrate terminal is left open $i_{PH(B)}$ flows through the device to the P^+ side to produce power. With P^+ held v_{PV} above the N Well, as in Fig. 2.19, this cell produces power. The $i_{PH(B)}$ current flows through the BJT, biasing it with Substrate as emitter, N Well as base and P^+ as emitter.

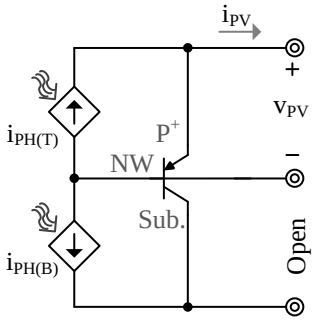


Fig. 2.19 Electrical model of P substrate open.

To produce maximum P_{PV} as in last case BJT operates in saturation. Thus most of $i_{PH(B)}$ after losing a portion as base current and all of $i_{PH(T)}$ forms i_{PV}.

Measurement: The cell produces maximum power of 3.9 µW, 26.7 µW and 128 µW, Fig. 2.20, about optimum voltages of 0.42 V, 0.46 V and 0.46 V at 1 klx, 10 klx and 80 klx. At 80 klx equivalent of direct sunlight, i_{PV} is around 278µA at $v_{PV(OPT)}$ of 0.46 V.

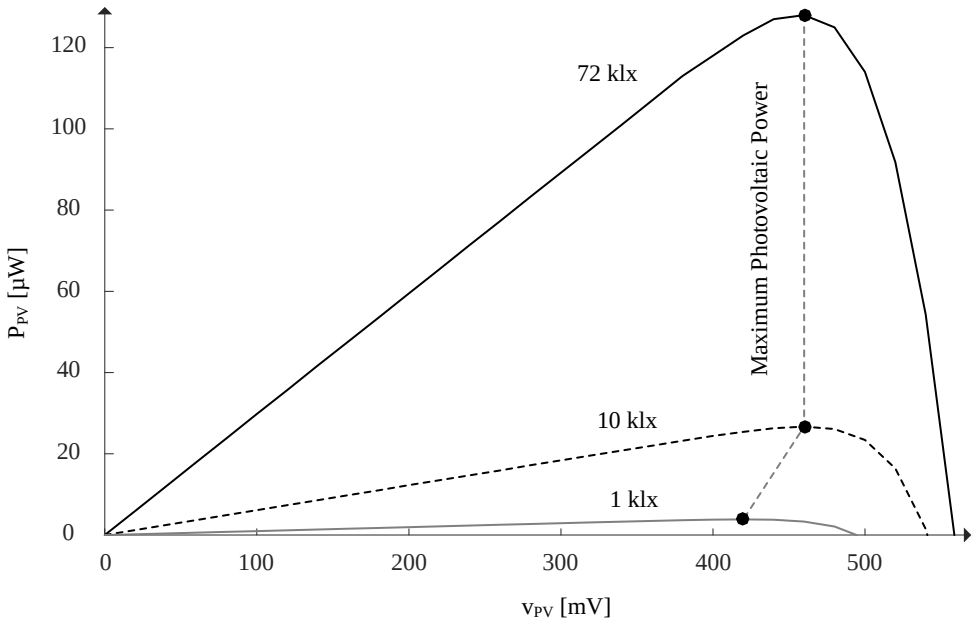


Fig. 2.20 Measurement of PV power across PV voltage of P substrate open.

2.4.4 Comparison

Power: Although not exactly the same, conventional N^+- and P^+-derived cells generated similar power. This is because their doping profiles are similar: both heavily doped and shallow. But because donor and acceptor atoms and the processing steps used to deposit them are not exactly alike, the P^+-derived PV cell produced 3× more power than the N^+ counterpart.

The cells that collected EHPs in the deeper well–substrate junction produced 5× to 7× more power, Table 2.1. One reason for this is longer diffusion length, because further-away EHPs can reach the depletion space. A wider depletion region is another factor because, with more atoms available, light frees more EHPs.

Table 2.1. Measured power from single-well 0.35-µm CMOS cells.

Single-Well PV Cells			$P_{PV(MPP)}$ [µW]		
			1 klx	10 klx	80 klx
N^+ in P Sub.			0.2	1.2	5.9
N Well in P Sub.			3.0	20	98
P^+ in N Well in P Sub.	Single Junction	P^+–N Well	0.4	3.1	18
		N Well–P Sub.	3.0	20	91
	Combined Junctions	Shorted	4.0	28	132
		Open P^+	4.0	28	132
		Open P Sub.	3.9	27	128

The standard stand-alone well–substrate cell produced 8% higher power at 80 klx than the bottom junction of the P^+–well–substrate device. Why this was the case at 80 klx and not at 1 or 10 klx may be current density. Since the physical structures are not *exactly* alike, parasitic resistances are different. As a result, higher substrate currents drop voltages that accentuate the effects of these differences on the depletion fields that collect EHPs to generate power.

Combined junctions produced more power than their isolated counterparts combined. The 18 and 91 µW that the top and bottom junctions of the P^+–well–substrate structure produced, for example, when isolated and exposed to 80 klx add to 117 µW, 23 µW less than the 132 µW the combined structure produced. This is because the same diffusion current the stand-alone structures lose to the diode the combined structure feeds to the opposing junction. Although some of it recombines in the well, much of it reaches the other junction. In other words, opposing junctions recover diode power.

Of combined junctions, the open-terminal configurations proposed require less metal. Eliminating the need to connect one terminal removes top-surface metal that would otherwise block light. With less metal, the cell receives more light, and as a result, produces more collectable EHPs. Plus, with less metal constraints, open-circuiting and partitioning P^+ into islands extend the depletion space to the sides of the islands to collect more EHPs. The cells prototyped for these experiments, however, connect all terminals to pins, so they do not reap these advantages. So removing the metal that connects to P^+ or substrate in the P^+–well–substrate prototype would generate more power than Table 2.1 show.

Outside of doping concentrations and diffusion depths, other processing factors affecting output power are passivation and silicided surfaces. Since these sit above the semiconductor, they filter some of the incoming light to liberate less EHPs. Keeping these layers off the surface of a CMOS PV cell raise output power, but not without increasing series resistance and risking some reliability.

MPP: The maximum power points (MPP) for the well–substrate and N^+- and P^+-derived cells were 0.50, 0.40, and 0.36 V, respectively. The voltage of the well–substrate cell is higher because doping concentration is lower, and the corresponding diode is therefore weaker. As a result, diode losses balance photonic gains at higher PV voltages. The maximum power points for the combined junctions were higher at 0.46 V than their constituent junctions at 0.36 and 0.38 V. This is probably because opposing junctions recover some diode power, so diode losses cancel photonic gains at a higher PV voltage. The maximum power point for the isolated well–substrate junction in the P^+–well–

substrate structure was lower at 0.38 V than for the stand-alone counterpart at 0.50 V. Why this is the case is not clear.

Integration: CMOS circuits normally connect the P substrate to the most negative potential to isolate components, or more to the point, to keep substrate P–N junctions from forward biasing. Of available configurations, only the isolated P^+–well junction in the P^+–well–substrate structure connects the substrate to the most negative potential. So only this cell can share the substrate with integrated CMOS circuits, which is the second lowest power-producing configuration tested.

Thankfully, sharing the substrate is normally undesirable because a tiny PV cell captures a very small fraction of the incoming light. As a result, artificial and obstructed lighting generates power levels that are too low to be practicable. This is why increasing the surface area of the cell is so critical, and why dedicating one die for the cell and stacking it above the circuit captures more light and outputs more power than integrating the cell into the circuit. Plus, dedicating a single-well die saves money because coarse-pitched single-well area costs less than finer-pitched multi-well real estate. These winnings often outweigh the conduction losses and cost of 10–100 mΩ intra-die connections and multi-die packaging [94].

2.4.5 Cascaded Cells

Of possible N-well CMOS PV cells, N^+ and N well in P substrate variations cannot disconnect from the substrate, so they have no isolated terminals with which to stack. The P^+ in N well cell is the only one that can stack. Unfortunately, however, each cell in the

stack leaks substrate and BJT currents whose losses reduce the gains that using multiple cells to drive a switched-inductor converter produces.

Design: Since PV cells are essentially current sources, the chief design challenge with connecting PV cells in series is managing current mismatches. The problem is that substrate and BJT currents between cells leak currents. In a stack like Fig. 2.21 shows, for example, the BJT current of the first cell i_{E1} and the substrate current of the second i_{S2} steal current from the first cell. So, to match currents, the photon current of the second i_{PH2} should be lower than that of the first i_{PH1}. Similarly, subsequent photon currents should be smaller than those of their preceding stages, so cell areas should be progressively smaller from the bottom to the top of the stack.

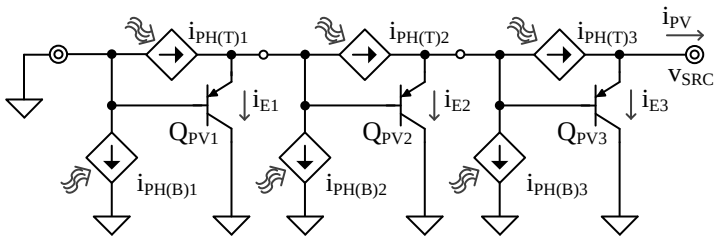


Fig. 2.21. Electrical model of three P^+ in N well CMOS PV cells stacked.

Still, imperfections across the die produce mismatches that are difficult to manage with cell area. Connecting dc–dc converters across each cell that ensure each cell voltage is optimum is one way of absorbing mismatches [95], except each converter dissipates power and requires space.

Stack Losses: Since absorption for higher wavelengths λ_{LIGHT} is lower, substrate currents and related losses usually overwhelm those of the BJT currents above roughly 490 nm [54]–[55]. This means i_S normally causes most cell-stack losses. So, since the

voltage at each intermediate connection (in Fig. 2.21) is the lower cell's emitter voltage v_E, which corresponds to the number of PV voltages the lower cells produce, P_{LOSS} reduces to roughly

$$P_{LOSS} \approx \sum_i i_{S(i)} v_{E(i-1)} \approx \sum_i i_{S(i)} (i-1) v_{PV} , \tag{2.6}$$

where each junction loses power. This means P_{LOSS} rises with the number of cells in the stack, as Fig. 2.22 shows when total chip area is 4 mm^2 and collectable power P_{PH} is 54 µW.

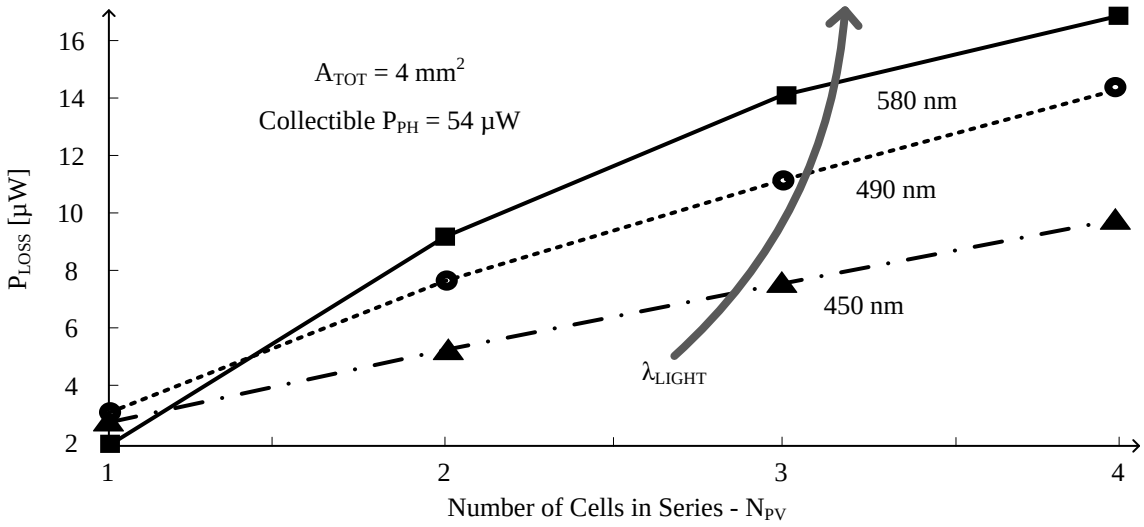


Fig. 2.22. Power losses across the number of cells stacked and wavelengths.

2.5 Other Photovoltaic Cells

2.5.1 Thin Film Single Junction

Thin film photovoltaic cells are PV cells made of materials that generate considerable power from light with material thickness of only few micrometres. Thin film materials have high light absorption coefficient as a result photons passing through them produces

EHPs at much higher rate and a result a short thickness of the material can absorb large incident photon densities that solar light provides [96]. For example to generate the same number of EHPs, N_{EHP}, thin film amorphous silicon material, Fig. 2.23, requires only 3 μm in comparison with crystalline silicon that needs 250 μm thickness.

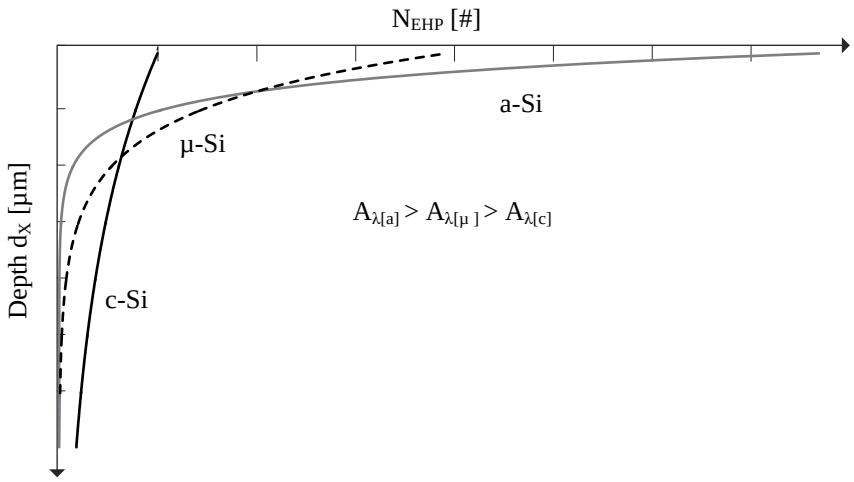


Fig. 2.23. Absorption profile of light for different Si materials.

The thin films cells, Fig. 2.24, materials deposit the active P-N junctions on glass substrate that provides the structural integrity for the cells. Thin film tend to have lower costs because of the thin material thickness and unified fabrication process unlike wafer processing that needs spate steps for crystal growth, wafer processing and cell processing [53]. The low thickness of these PV cells allows for flexible cells that enables more applications. The deposition of semiconductor materials on glass substrate enables multiple cells on the same substrate that can connect in series. The typical low cost techniques in these technologies have to allow separation around 300 μm but with more investment even separation of 10 μm are possible [97].

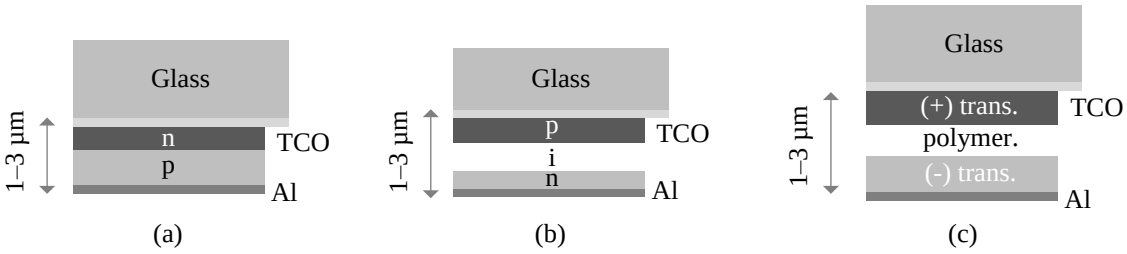


Fig. 2.24 Thin film cells (a) non-Si (b) a-Si (c) organic

2.5.1.1 Amorphous Silicon

Among the silicon thin film options amorphous silicon is the most prominent. In comparison with crystalline silicon, the amorphous material lacks long range crystalline order and when untreated has dangling bonds that capture large carriers and reduce diffusion length. In essence the imperfections allow a larger absorption coefficient, however also limits diffusion length and collection ability. Hydrogenating the cells allow for passivating the dangling bonds and increasing efficiency. However, after short time exposure the efficiency degrades to a lower value. The highest efficiency report for single junction amorphous PV cells is around 10% [67].

The structure of the amorphous cell in Fig. 2.24b has an intrinsic region between the P and N -type regions, the intrinsic region essentially extends the depletion region in the PN junction by the intrinsic depth and therefore increase the collection probability. The amorphous silicon structure consists of a glass substrate with a transparent conducting oxide (TCO) providing the front contact, a p-i-n structure follows and the bottom aluminium contact completes the cell. Small areas serially connect to produce large modules. The amorphous silicon cells can have low thickness between 300 nm and 3 µm of active area and application based glass substrate thickness.

2.5.1.2 Non-Silicon

With dip in availability of silicon with large number of wafer based products, has enabled thin film cells made of non-Si technologies, Fig.2.24c. Cadmium tellurium (CdTe) and copper-indium selenide (CIS) are the prominent non-Si technologies available today. The latest cells have efficiency around 21% inching towards efficiency of crystalline silicon cells. The thickness of these cells is typically 1–3 μm. These cells are 30% – 40% lower cost than crystalline silicon cells making it attractive. The disadvantages of these cells are the requirement of larger area for the same power density as wafer based cells.

The structure of these cells include a glass substrate, transparent conducting oxide, a layer of CdS, the CdTe or CIS layer and metallic back contact, Fig. 2.24c. The Cd in these cells are toxic and be a detriment to it widespread usage, especially the CdTe cell. Among these cell CdTe cell is slightly cheaper than CIS.

2.5.1.3 Organic

One of the emerging thin film photovoltaic technologies is organic photovoltaics (OPVs), with the advantages of being light and flexible. It can be conformed to different shapes makes it attractive to many application. Organic PV cells use organic materials for light absorption and charge transport. One advantage of organic cells is the ability for molecular engineering that enable adjusting the bandgap and tune for the light wavelength of the application. Like other technologies the high absorption coefficient enables the depth to be just few hundred nanometres. However it has low efficiency of 11% of recent cells and is less stable in comparison with crystalline silicon [67].

In organic photovoltaic cell large conjugated system of carbon based molecules absorb light. In these cells the lowest unoccupied molecular orbital (LUMO) serve as conduction band, and the highest occupied molecular orbital (HOMO) serve as the valence band. The energy gap between HOMO and LUMO serves as the bandgap in organic materials. When light passes through the material, the molecules absorb photons and reach an excited state. When these excitons are exposed to electric field the excitons are broken up to create EHPs.

Bilayer organic PV cells have hole transport layer and electron transport layer and the work function difference between the layers generate the electric field of EHP generation. The lower efficiency and lower mobility for charge transport are challenge that needs to be addressed. Similarly a stability of organic cells under long time exposure is also one of the challenges in the current research.

2.5.2 Stacked

Stacked cells use multiple PN junctions of varying bandgaps that connect in series to effectively absorb the different wavelengths of light, in Fig. 2.25.

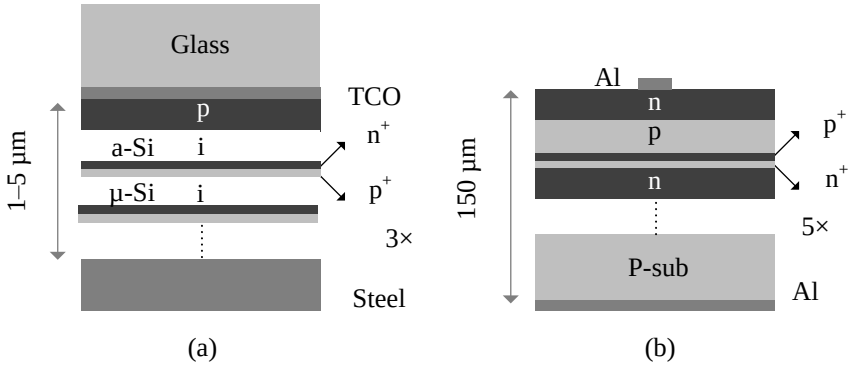


Fig. 2.25. Stacked PV cells (a) silicon (b) Non-silicon.

The thin film technologies with their lower material thickness and fabrication cost adapt naturally to stacked cells. Between each PN is layers of highly doped NP junction that acts a tunnel diodes, where the low thickness highly doped N and P layers sandwiched between PN junctions allow for the electron and holes to tunnel through the NP region with minimum voltage drop, Fig. 2.26. The mismatch between these stacked cells can lead to current mismatch losses.

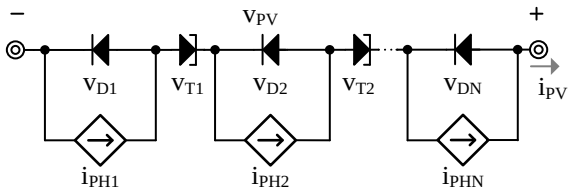


Fig. 2.26. Electrical model of stacked PV cells.

2.5.3 Comparison

The different options of PV technologies have their unique advantages. Custom crystalline silicon are most prominently used but recently thin film cells are generating lot of penetration, other emerging technologies like OPVs are also showing a lot of progress. In microsensors the trade-off between area that defines footprint of the sensor and cell price that determines the total sensor cost are important parameters. In cost considerations thin film PV cells are cheaper but need higher footprint in comparison to crystalline cells and are toxic, CMOS cells that fabricate from the same process that develop the sensor circuitry has the benefits of low cost due the scale of production and reuse of technology that fabricates the sensor.

Table 2.2 Approximate performance comparison of various PV technologies.

Approximate Performance				Active Depth [µm]	Power [µW]	η_{PV} [%]	Cost	d_S [mm]
Crystalline Silicon (c-Si)	CMOS	N^+/PSub.	Epi	20	6	0.6	$$$	1
			Non	250	10	1		1
		NW/PSub.	Epi	20	98	9.8		1
			Non	250	160	16		1
		P^+/NW/PSub.	Epi	20	18–90	1.8–9		1
			Non	250	30–145	3–15		1
			Comb.	250	240	24		1
	Custom			250	252	25	$$$$	1
Thin film	a-Si			1–3	100	10	$$	0.3
	Organic			1	112	11	$$	0.5
	Non-Si			1–3	210	21	$–$$	0.3
Stack	a-Si/µ-Si			1–5	136	14	$$$$$	–
	Non-Si			150	388	39		–

Although amorphous silicon costs less than crystalline single-well complementary metal–oxide–semiconductor (CMOS) [67], single-cell CMOS cells generate 10%–13% higher power, Table 2.2. Multi-well CMOS junctions generate more power than single-well junctions [67], but require additional steps in the fabrication process, so they cost more. Custom mono-crystalline cells output as much as single-well cells and custom multi-junction non-silicon cells can output 10%–15% more, but investing to establish and maintain a custom fabrication facility is not always possible.

2.6 Summary

Since lower doping concentrations extend diffusion lengths and depletion regions, the prototyped 0.35-μm single-well CMOS N well–P substrate PV cell generates 5× more power at 91–98 μW than P^+ in N well at 18 μW when exposed to the equivalent of direct sunlight. Two-junction cells generate 7× more power at 128–132 μW than P^+ in N well and 31%–45% more power than N well in P substrate. The configuration proposed that opens the P^+ terminal to combine the shallower and deeper junctions eliminates top-surface metal from the structure, so more light can penetrate to generate even more power. Although using the substrate junction keeps the proposed structures from sharing the substrate with a CMOS circuit, sharing the substrate is normally undesirable. Since microsystems can only avail a few millimeters, dedicating one die to the PV cell and stacking it above the CMOS circuit produces much more power than placing the PV cell alongside the circuit, especially when drawing power from multiple junctions. Plus, using a coarser single-well CMOS cell costs less than its finer and multi-well counterparts. Custom mono-crystalline cells output as much as single-well CMOS cells and custom multi-junction non-silicon cells can output 10%–15% more, but investing to establish and maintain a custom fabrication facility is not always possible.

CHAPTER 3. CHARGER–SUPPLY CIRCUITS

A millimeter-scale light-energy harvesting system typically accommodates a PV cell and on-board battery to supply microsensor loads. The photovoltaic cell produces maximum power at an optimum voltage $v_{PV(MPP)}$, 0.2–0.6 V, that varies with lighting conditions [68]. On the other hand, the chemistry of the batteries fixes its operating voltage, for example, 2.7–4.2 V for Li ion cells and, 0.9–1.6 V for Ni-Cd cells. Similarly, the sensor load requires a regulated supply voltage that ensures optimum performance, say 1V. Therefore, a circuit that can transfer power between the PV cell, battery, and the load, all of which operate at different voltage levels, is a fundamental requirement of the system. Since all the power sources and loads operate at DC voltages, a DC–DC converter can serve as the power-transfer-circuit.

3.1 Power Transfer Circuits

Three prominent categories of DC–DC converters are linear regulators [38], switched-capacitors [98]–[100] and switched-inductors [88]–[99]. The linear regulators modify the conductance of a power switch between input and output to transfer power between different voltages. The switched capacitors and inductor circuits use capacitors and inductors as an intermediate stage to store and release energy from and to different voltage levels.

3.1.1 Linear Regulators

3.1.1.1 Operation

Linear regulators transfer energy from input v_{IN} to output v_O by modulating the resistance and therefore the voltage drop across the pass switch M_P. With the voltage drop across M_P the output voltage is always less than input, therefore this circuit cannot boost. The series switch continuously conducts the load current as a result for a steady load current the output current is same as input current and has minimal high frequency component. In Fig. 3.1, the feedback resistor shunt samples the output voltage as v_{FB}. The error amplifier EA_O further amplifies the error between v_{FB} and target reference voltage v_{REF} to generate the drive signal for the pass transistor the inverting gain single transconductance amplifier M_P completes the negative feedback loop that regulates the output.

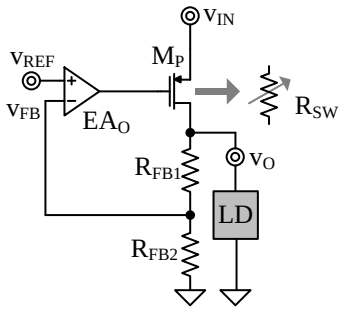


Fig. 3.1. Linear regulator circuit.

3.1.1.2 Efficiency

The major loss in linear regulator circuit is the loss across the series pass switch. The input power $v_{IN}i_{IN}$ incurs an ohmic loss of $v_{SW}i_{IN}$ before reaching the output as v_Oi_{IN}. Here v_{SW} the voltage drop across switch is the difference between v_{IN} and v_O and is

typically greater than 200 mV. Lower than 200 mV v_{SW} values can push the M_P into linear region and cause the drop in gain of the negative feedback loop and as a result reduces the output regulation ability. A secondary loss in the linear regulator is quiescent power $v_{IN}i_Q$ consumed by the controller that includes the error amplifier buffer and feedback path. The efficiency of the linear regulator circuit:

$$\eta_X = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_Q} = \frac{v_O i_{IN}}{v_{IN}(i_{IN} + i_Q)}, \tag{3.1}$$

improves with low v_{SW} values as well as with lower quiescent currents. However since input and output voltages are application dependent the v_{SW} is a given. The quiescent power can scale with load power to scale efficiency with load at cost of regulation bandwidth; here transient feed forward paths can help the circuit to react to sudden load dumps.

3.1.2 Switched-capacitor circuits

3.1.2.1 Operation

Switched-capacitor circuits transfer energy from input v_{IN} to output v_O by first charging one or multiple capacitors from the input then reconfiguring the capacitors discharging the combination to the output. The circuit operates in two phases to transfer energy the parallel charge phase and the series discharge phase as the Fig. 3.2 shows. In the charge phase capacitors C_{F1} to C_{FN} connect in parallel to charge each of the capacitor to voltage $v_H - v_L$ and in the series discharge phase the capacitors connect in series to charge v_H' to $v_L'+N_X(v_H - v_L)$. For example with v_H and v_L' as the input, v_H' as the output and v_L at ground the circuits boost v_{IN} to (N_X+1) v_O.

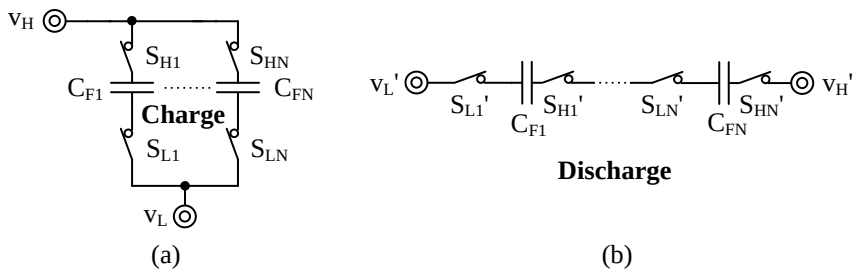


Fig. 3.2. Switched-capacitor circuit (a) parallel charge (b) series discharge.

As an example the switched-capacitor (SC) doubler circuit in fig 3.3, transfers energy, by first charging a flying capacitor C_{FLY} in parallel with input capacitor C_{IN} from the input voltage v_{IN}, and then discharging C_{FLY} by connecting it in series between C_{IN} and the battery $v_{BAT.}$ The input source in this example models the photovoltaic current. The SC circuit in Fig. 3.3a, connects the capacitor C_{FLY} in parallel with C_{IN} by closing switches S_{E1} and S_{E2}. v_{IN} initially dips in Fig. 3.3b, when the C_{IN} shares charge with C_{FLY} in parallel, then i_{IN} charges both C_{FLY} and C_{IN} for the charging period, which is half of the switching period t_{SW}. Further, the circuit closes switches S_{DE1} and S_{DE2} to connect the series-stack of C_{FLY} and C_{IN} to the battery. v_{IN} dips again during the initial charge sharing phase, i_{IN} then charges the output by discharging $C_{FLY,}$ while at the same time charging C_{IN}. This way the circuit in Fig. 3.3a can boost v_{PV} to a maximum of double the value. By charging more capacitors in parallel, and then connecting all of them in series can boost v_{IN} to higher voltages [47]. To transfer energy between fixed voltages at input and output the circuit switches more frequently to deliver higher power.

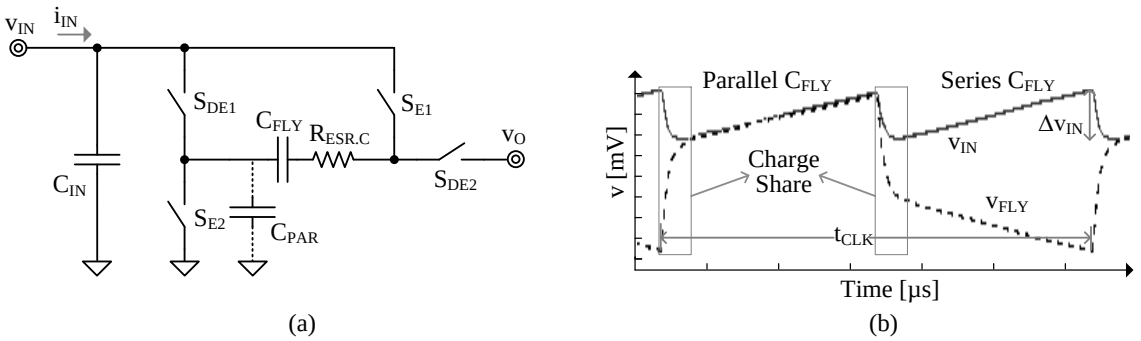


Fig. 3.3. Switched-capacitor doubler (a) Circuit model (b) simulated waveforms.

3.1.2.2 Efficiency

In the case of the flying capacitor with initial voltage $v_{FLY.IN}$ connecting to a voltage source v_{IN} in the charging phase, the voltage source v_{IN} supplies is:

$$E_{IN} = v_{IN}Q_{IN} = v_{IN}C_{IN}(v_{IN} - v_{FLY.IN}). \tag{3.2}$$

The flying capacitor accumulates the difference between its initial energy $E_{FLY.INI}$ and the final energy $E_{FLY.FIN}$ over the charge cycle as:

$$E_O = E_{FLY.FIN} - E_{FLY.INI} = 0.5C_{FLY}v_{IN}^{\ 2} - 0.5C_{FLY}v_{FLY.IN}^{\ 2}. \tag{3.3}$$

The switch dissipates the difference between E_{IN} and E_O as conduction energy loss:

$$E_R = E_{IN} - E_O = 0.5C_{FLY}(v_{IN} - v_{FLY.IN})^2 = 0.5C_{FLY}\Delta v_{FLY}^{\ 2}. \tag{3.4}$$

The switch capacitor circuit also losses gate charging energy turning on and off the switches:

$$E_G = C_{EQ}\Delta v_G^{\ 2} \tag{3.5}$$

In an on-chip implementation, C_{FLY} introduces a parasitic bottom-plate capacitor C_{PAR} (at roughly $0.1C_{FLY}$ [98]). C_{PAR} charges and discharges every cycle, without transferring the energy it accumulates to the battery, but instead dissipating it across the switches. As a result the ohmic losses for the on-chip implementation $P_{R(INT)}$ is higher than the off-chip case $P_{R(EXT)}$. The flying capacitors in the SC circuit incur as ripple Δv_{FLY} ripple across it transfer charge q_{FLY} every cycle f_{SW} and deliver output power $v_O q_{FLY} f_{SW}$. So to transfer more power the either Δv_{FLY} needs to increase or f_{SW} needs to increase. Higher switching frequency f_{SW} can reduce conduction losses by reducing Δv_{FLY} to but at the cost of higher gate-drive losses. Overall as the number of switches and flying capacitors increase for higher boosting and bucking ratios so does the losses in the circuit and the efficiency at high power level reduces for N-stage circuit with quiescent controller current i_Q reduces to:

$$\eta_X = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_L} = \frac{v_O}{N_X v_{IN} + v_O i_Q} \tag{3.6}$$

3.1.3 Switched-inductor circuits

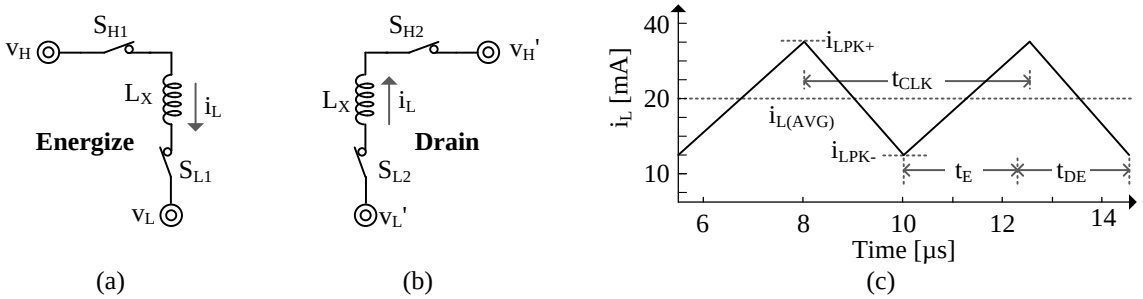
3.1.3.1 Operation

A switched-inductor circuit transfers power, by energizing an inductor from the photovoltaic cell and then de-energizing it to the battery. In Fig. 3.4a, switch S_{H1} and S_{L1} closes, to energize the inductor L_X across the energizing voltage $v_H – v_L$ from $i_{L.PK-}$ to $i_{L.PK+}$ during the energizing time t_E to draw energy from v_H and store energy in the inductor. The de-energizing voltage v_{DE} or ($v_H' – v_L'$) drains the inductor during the time

t_{DE} to transfer energy to v_H'. With v_H as input v_{IN}, v_H'as the output v_O and v_L and v_L' at the ground, the circuit can buck or boost from v_{IN} to v_O:

$$d_X = \frac{v_O}{v_{IN}} = \frac{t_E}{t_{DE}} \tag{3.7}$$

This way the switched-inductor (SI) circuit can buck or boost between any two sets of input and output voltage with just 2–4 switches. Similar to the SC circuit SI circuit also incurs ohmic losses across series path resistances and gate-drive losses turning on/off the switches. However with less number of switches the switch inductor converter can potentially have lower power stage losses, simpler control, as a result lower controller power.



(a) (b) (c)

Fig. 3.4. Switched-inductor circuit (a) energizing (b) drain (c) simulation.

To further explore the potential of SI circuits for harvesting energy from the PV cell, Section 3.2 evaluates the losses in SI circuit to decide the optimal control for most efficient energy transfer.

3.2 Low Power Operation

3.2.1 Conduction Mode

In the context switched-inductor power transfer circuits, to transfer power between a source and load that operate at different voltages, the circuit energizes and drains L_X in the alternate phases of the switching cycle. There are two traditional mode of operations for switched-inductor circuits are continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [38], [99] and [100]. In CCM, the inductor continuously flows current while the energizing voltage ramps the current up and de-energizing voltage ramps the current down to the same extent successively, as in Fig 3.4.c.

In low power operating region the average inductor current I_L that sets the average input and output current is quite low as a result energizing and de-energizing for low periods of time can create a large current ripple Δi_L and large Δi_L across a small I_L can push the current to a negative value. A negative current in this case would lead to power flow opposite to the intended direction, and as a result discharge the output instead of charging it. On the other hand short energizing and de-energizing time will lead to short switching times and large switching frequency and as a result excessively large switching losses. For example a 100-µH inductor with 1 V energizing and de-energizing voltage will have to switch at more than 1 MHz for keeping Δi_L below 5 mA and 100 MHz for Δi_L below 50 µA.

Fortunately energizing the inductor to a peak current and disconnecting the de-energizing voltage when the i_L goes to zero allows for transfer of large packet of energy while switching at a much lower frequency and without output discharge Fig. 3.5. This way, in

discontinuous-conduction mode (DCM) [90]–[95], L_X transfers a large energy packet E_{IN}. Since i_L reflects how much energy L_X stores, E_{IN} in the case of Fig. 3.5a is the energy in L_X at the end of the energizing period t_E, when i_L peaks at $i_{L(PK)}$:

$$E_{IN} = 0.5 L_X i_{L(PK)}^2 \tag{3.8}$$

that, across a long clock period t_{CLK}, delivers microwatts. Since $i_{L(PK)}$ is higher for larger packets, t_E and t_D can be longer and sufficiently infrequent to keep switching losses low [].

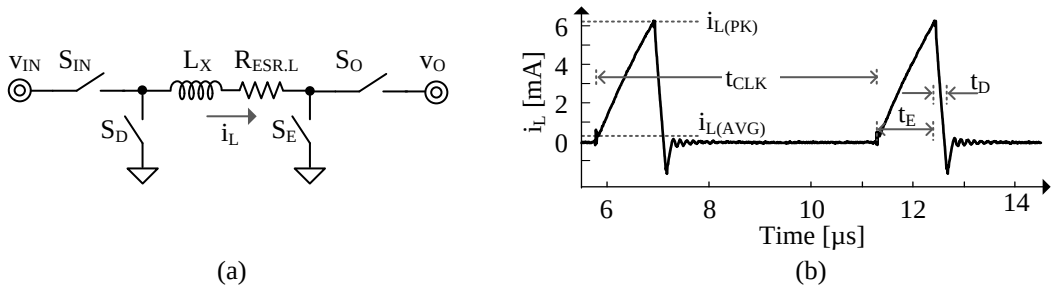


Fig. 3.5. Switched-inductor (a) circuit (b) simulated inductor current in DCM.

The size and frequency of the energy packets that L_X delivers sets how much power v_{IN} sources with P_{IN}:

$$P_{IN} = \frac{E_{IN}}{t_{CLK}} = E_{IN} f_{CLK} \tag{3.9}$$

For this, S_{IN} and S_E in Fig. 3.5a impress v_{IN} across L_X long enough across t_E to raise i_L to $i_{L(PK)}$:

$$t_E = \frac{L_X i_{L(PK)}}{v_{IN}} \propto i_{L(PK)}, \tag{3.10}$$

which means t_E rises with $i_{L(PK)}$. S_D and S_O similarly impress $-v_O$ across L_X long enough across t_D to reduce i_L from $i_{L(PK)}$ to zero:

$$t_D = \frac{L_X i_{L(PK)}}{v_O} \propto i_{L(PK)}, \tag{3.11}$$

so t_D also scales with $i_{L(PK)}$. In fact, since L_X's equivalent series resistance R_{ESR} conducts i_L only across t_E and t_D, S_{IN} and S_E only across t_E, and S_D and S_O only across t_D, all conduction times t_{ON} similarly rise with $i_{L(PK)}$:

$$t_{ON} = \left\{ \begin{matrix} t_E + t_D & \text{for } R_{ESR} \\ t_E & \text{for } S_{IN}, S_{GE} \\ t_D & \text{for } S_O, S_{GD} \end{matrix} \right\} \propto i_{L(PK)} \tag{3.12}$$

3.2.2 Losses

The switched-inductor incurs ohmic losses transferring power across series path resistances, gate-drive losses switching on/off the power switches and across the controller.

3.2.2.1 Ohmic

Like switches, L_X's R_{ESR} dissipates ohmic energy E_{ESR} when R_{ESR} conducts i_L across a t_{ON} fraction of t_{CLK}:

$$E_{ESR} = {i_{L(RMS)}}^2 R_{ESR} t_{CLK} = \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 R_{ESR} t_{ON} \propto {i_{L(PK)}}^3. \tag{3.13}$$

And since t_{ON} rises with $i_{L(PK)}$, E_{ESR} is proportional to ${i_{L(PK)}}^3$. In other words, E_{ESR} rises more quickly with $i_{L(PK)}$ than $E_{SW(MIN)}$ does.

3.2.2.2 Quiescent

Portions of the controller operate continuously across t_{CLK}, so energy $E_{C(DC)}$ changes with t_{CLK}:

$$E_{C(DC)} = P_{C(DC)}t_{CLK}. \tag{3.14}$$

Others need only engage when L_X conducts, so they may consume power a t_{ON} fraction of t_{CLK}. Energy $E_{C(DUTY)}$ for these duty-cycled blocks therefore changes with t_{ON}, and as a result, $i_{L(PK)}$, but not t_{CLK}:

$$E_{C(DUTY)} = P_{C(Q)}\left(\frac{t_{ON}}{t_{CLK}}\right)t_{CLK} = P_{C(Q)}t_{ON} \propto i_{L(PK)}\,. \tag{3.15}$$

Still others need only engage momentarily, when transitioning between switching states. These transient blocks consume power across a constant period t_{TRAN}, so energy $E_{C(TRAN)}$ is independent of both t_{CLK} and t_{ON}, and as a result, also of $i_{L(PK)}$:

$$E_{C(TRAN)} = P_{C(Q)}\left(\frac{t_{TRAN}}{t_{CLK}}\right)t_{CLK} = P_{C(Q)}t_{TRAN} \neq f(i_{L(PK)}) \tag{3.16}$$

3.2.3 MOS Switch Design

Ideal switches occupy no space, drop no voltage, leak no current, and respond instantly. In practice, however, switches occupy space and incorporate resistance, capacitance, and leakage paths. So in addition to requiring space, they also drop voltages, leak currents, and require time to respond [100]–[121].

MOSFETs: NFETs and PFETs in Fig. 3.6a–b are *synchronous* devices because they transition between on–off states when prompted by synchronizing gate signals. They can drop 10–200 mV in the on state and respond in nanoseconds. Since current can flow

in both directions, either terminal can serve as the *source*. In the off state, their body diodes can always conduct current: substrate NFETs from the grounded substrate and welled PFETs into the well.

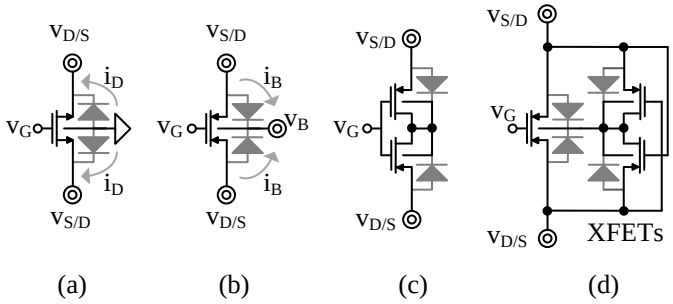


Fig. 3.6. (a) Substrate, (b) welded, (c) in-line, and (d) off-line FETs.

Blocking MOSFETs: Isolating the bulk of welled FETs, and blocking the bulk path with opposing diodes keep body diodes from leaking current. The body diodes of the in-line pair M_{P1}–M_{P2} in Fig. 3.6c, for example, block one another, so they cannot conduct. This way, when M_{P1}–M_{P2} close, switch terminals bias the bulk v_B within mV's of their terminal potentials. And when M_{P1}–M_{P2} open, bulk capacitance holds v_B, or if either switch terminal rises, the diode attached to that terminal raises and biases v_B to the higher potential.

With the body always biased close to the higher potential, the welled FETs do not suffer bulk effect when conducting. However, two switches offer twice 2× the resistance or twice 2× the capacitance of one switch. This is a drawback because higher resistance burns more ohmic power and higher capacitance requires more gate-drive power [101].

Biasing the bulk with off-line FETs eliminates the second in-line FET. Off-line cross-coupled pair M_{X1}–M_{X2} in Fig. 3.6d, for example, biases M_P's bulk v_B to the highest potential: M_{X1} to $v_{S/D}$ when $v_{S/D}$ exceeds $v_{D/S}$ and M_{X2} to $v_{D/S}$ otherwise. The drawback is that M_{X1}–M_{X2} are off when terminal voltages are within a threshold of one another, so body diodes bias v_B to the higher potential. This means, v_B may not rise as quickly as the higher potential. Fortunately, this is only momentary.

Asynchronous Switches: Diodes and diode-connected FETs in Fig. 3.7a–b are *asynchronous* because they close and open automatically when current flows and reverses. In other words, they do not require a synchronizing signal. They can drop 0.5–0.7 V in the on state and respond in nanoseconds.

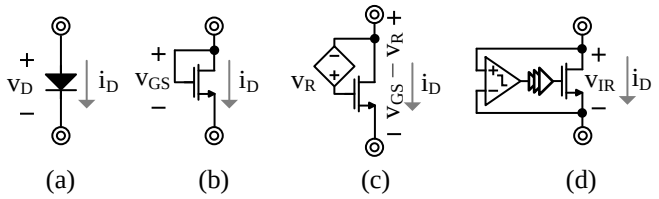


Fig. 3.7. (a) Diode (b) MOS diode (c) threshold adjusted (d) comparator-synchronized.

Threshold-shifted [38] and comparator-synchronized [38] FETs in Fig. 3.7c–d can drop much lower voltages. But since matching and tracking a threshold voltage v_T across process and temperature is less accurate than sensing a voltage difference, comparator-synchronized FETs drop lower voltages. The drawback is that the comparator requires μW's to respond within 1 μs [102]. Still, the mW's saved with a lower voltage drop outweigh the μW's lost in the comparator.

3.2.3.1 Switch Loss

Transistors consume ohmic power P_R when they conduct and require gate-drive power P_G to switch between states [101]. Interestingly, resistance falls and capacitance climbs with wider channels. So channel widths should be just high enough for the rise in P_G to cancel the fall in P_R [101]. And channel lengths should be as short as possible because both resistance and capacitance climb with channel length.

Switches in the network dissipate ohmic energy E_R when they conduct i_L. Since i_L is nearly a triangle across every instance of t_{ON}, $i_{L(RMS)}$ across t_{ON} is $i_{L(PK)}/\sqrt{3}$ [101]. So the power P_R consumed by the resistance of a switch R_{SW} is $i_{L(RMS)}{}^2 R_{SW}$ across the t_{ON} fraction of t_{CLK} that R_{SW} conducts i_L. So E_R, which is P_R across t_{CLK}, is

$$\begin{aligned} E_R &= \left[i_{L(RMS)}{}^2 R_{SW} \left(\frac{t_{ON}}{t_{CLK}} \right) \right] t_{CLK} = \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 R_{SW} t_{ON} \\ &= \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 \left(\frac{\rho_{SW} L_{SW}}{W_{SW}} \right) t_{ON} \end{aligned} . \tag{3.17}$$

In the case of MOS switches, R_{SW}, and as a result, E_R fall with decreasing channel resistivity ρ_{SW} and channel length L_{SW} and increasing channel width W_{SW}.

Unfortunately, MOS switches also require gate-drive energy E_G to control them. E_G, to be more specific, is the energy that the gate capacitance C_G requires to charge across its gate-drive voltage Δv_G:

$$E_G = C_{EQ} \Delta v_G{}^2 = (C_{OX}'' L_{SW} W_{SW}) \Delta v_G{}^2 . \tag{3.18}$$

Here, of course, C_G, and as a result, E_G rise with oxide capacitance per unit area C_{OX}'', W_{SW}, and L_{SW}.

Since both E_R and E_G fall with shorter lengths, L_{SW} should be the minimum length L_{MIN} possible. But because E_R falls and E_G rises with increasing W_{SW}, W_{SW} should neither be short nor wide. Instead, designers should raise W_{SW} until the rise in E_G cancels the fall in E_R. In other words, E_R and E_G are at their lowest combined point when W_{SW} is optimal width W_{SW}':

$$\left.\frac{\partial E_R}{\partial W_{SW}} + \frac{\partial E_G}{\partial W_{SW}}\right|_{W_{SW}'=\sqrt{\frac{i_{L(PK)}{}^2 t_{ON}\rho_{SW}}{3C_{OX}''v_G{}^2}}} = 0. \tag{3.19}$$

With L_{MIN} and W_{SW}', E_R' equals E_G', and together, they yield $E_{SW(MIN)}$:

$$E_{SW}' = E_R' + E_G' = 2E_G' \propto \sqrt{i_{L(PK)}{}^2 t_{ON}} \propto i_{L(PK)}{}^{1.5} \tag{3.20}$$

And since t_{ON} scales with $i_{L(PK)}$, $E_{SW(MIN)}$ rises with $i_{L(PK)}{}^{1.5}$.

In practice, gate signals across the circuit crisscross during transitions. As a result, adjacent switches momentarily short the inputs and outputs to which they connect. This is a problem because, when optimized like just described, resistances are so low that they can burn excessive power when they short. This is why designers insert dead-time periods between the gate signals of adjacent switches [105].

3.2.4 Fractional Loss

Switched inductors in discontinuous conduction can either fix peak current $i_{L(PK)}$ and adjust frequency f_{CLK} [102]–[104] or fix f_{CLK} and adjust $i_{L(PK)}$ [109]–[117] to adjust power level. Of the two schemes, the one with the lowest fractional losses E_{LOSS}/E_{IN}, as concluded earlier, produces the highest power-conversion efficiency η_C. To determine this, first note E_{ESR}/E_{IN} rises with $i_{L(PK)}$ and $E_{SW(MIN)}/E_{IN}$ falls with $1/i_{L(PK)}{}^{0.5}$ and

$E_{C(DUTY)}/E_{IN}$ and $E_{C(TRAN)}/E_{IN}$ fall faster with $1/i_{L(PK)}$ and $1/i_{L(PK)}^2$, as Fig. 3.8 shows. So like in the case of W_{SW}, designers should raise $i_{L(PK)}$ until the rise in E_{ESR}/E_{IN} cancels the drops in $E_{SW(MIN)}/E_{IN}$, $E_{C(DUTY)}/E_{IN}$, and $E_{C(TRAN)}/E_{IN}$. Note that $E_{C(DC)}/E_{IN}$ reduces to $P_{C(DC)}/P_{IN}$ and is therefore independent of $i_{L(PK)}$. In other words, fixing $i_{L(PK)}$ to its optimal setting $i_{L(PK)}'$ and adjusting f_{CLK} is the scheme that produces the highest efficiency, irrespective of E_{IN}. And since W_{SW}' depends on $i_{L(PK)}$, W_{SW}' for $i_{L(PK)}'$ is optimal for all values of E_{IN}.

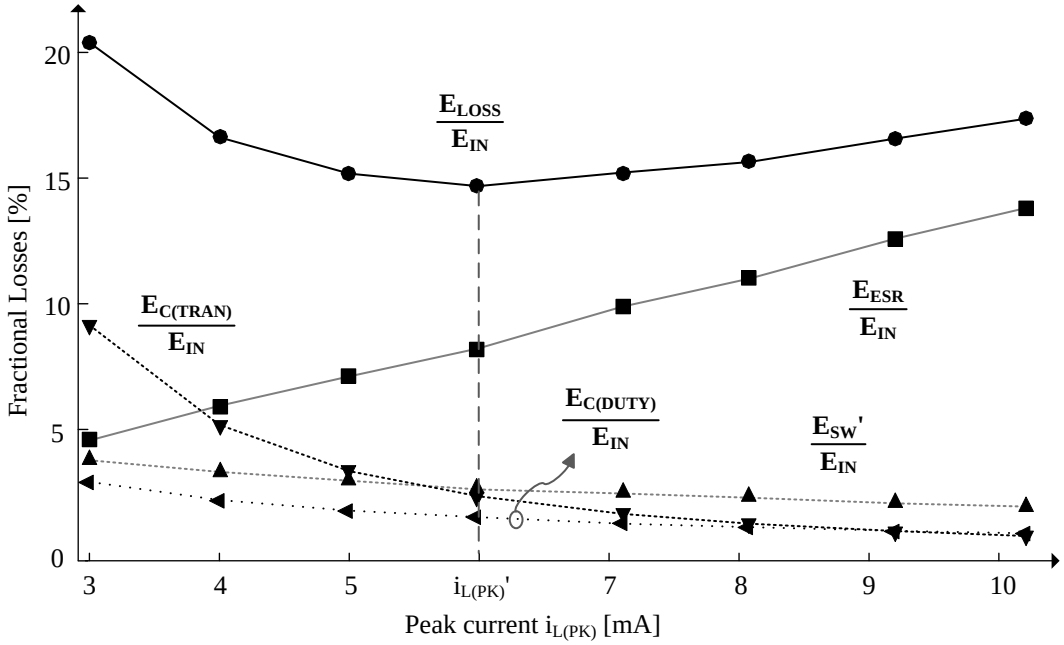


Fig. 3.8. Simulated fractional losses.

3.2.5 Transfer Scheme

3.2.5.1 Variable-Peak/Fixed-Frequency

In discontinuous conduction mode, the power transfer is directly proportional to the size of the energy packet and how frequently they transfer. In variable peak fixed frequency

scheme the clock time period t_{CLK} is fixed but the peak inductor current $i_{L(PK)}$ and thereby the size of the energy packet changes in response to change in the transferred power P_O. One advantage of this scheme is controlled frequency spectrum at the output as frequency content barely varies. The output regulation is also consistent as the minimum time period of response to a change is fixed.

In the Fig. 3.9 to transfer 75-µW load power the inductor current rises to 6.5 mA every 24 µs. When the load power rises to 120 µW the system continues to deliver the packets at the same frequency, however the controller changes the peak current of the inductor to 8.2 mA.

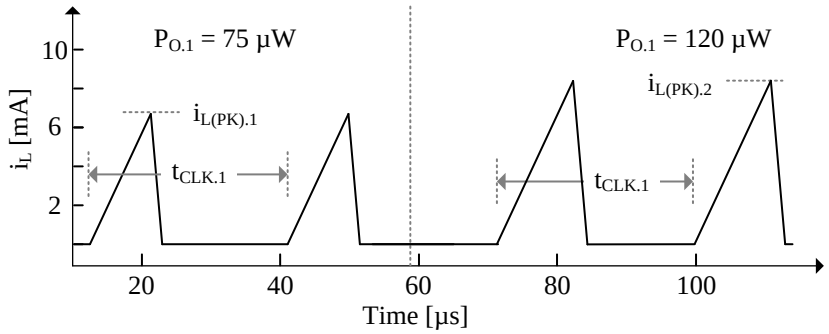


Fig. 3.9. Variable-Peak/Fixed-Frequency waveform.

Figure 3.10 illustrates the power-conversion efficiencies η_X of a 0.3-to-1.8-V boost 0.18-µm CMOS converter with a 47-µH–5.6-Ω inductor in discontinuous conduction with a variable size packet across 40–250 µW input power. At f_{CLK} of 80 kHz the efficiency peaks at 120 µW, however η_X falls above and below these points with the controller switches losses dominating below 120 µW and inductor ESR losses dominating above the power level. Among the 40, 80 and 120 kHz the 120 kHz option has the highest peak efficiency as its optimum efficiency is at higher power level. In

systems where the input source generally provides energy within a short power range this scheme is attractive.

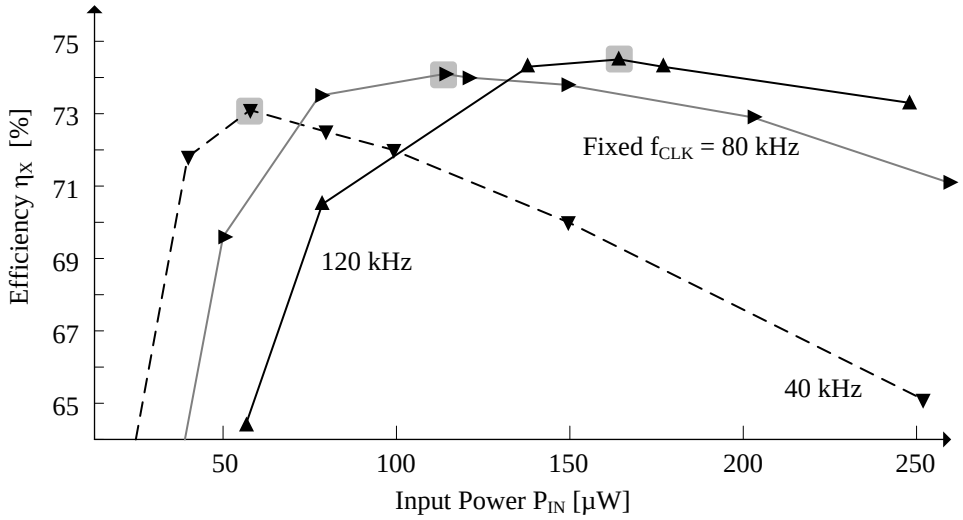


Fig. 3.10. Measured efficiency for fixed-peak and fixed-frequency schemes.

3.2.5.2 Variable-Frequency/Fixed-Peak

In the variable frequency fixed peak scheme, the inductor current peak is constant but frequency varies to change the power delivery, as in Fig 3.11. The frequency spectrum of this operation depends on the load level and can affect applications especially the once sensitive to EMI.

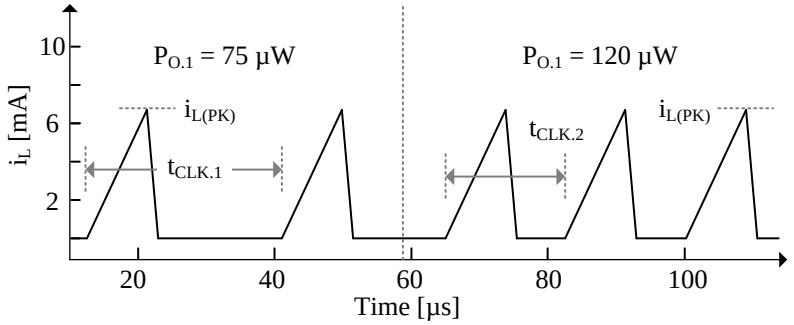


Fig. 3.11. Variable-Frequency/Fixed-Peak waveform.

In the Fig. 3.11 to transfer 75-µW load power the inductor current rises to 6.5 mA every 24 µs. When the load power rises to 120 µW the system continues to deliver same size packets, however the controller changes the duration between packets to 18 µs.

For the 47-µH–5.6-Ω inductor with $i_{L(PK)}$ fixed at 5, 6, and 10 mA, η_C is nearly flat above 50 µW. This results because E_{ESR}, $E_{SW(MIN)}$, and $E_{C(DUTY)}$ both scale with E_{IN} and overwhelm $E_{C(DC)}$ and $E_{C(TRAN)}$, so fractional losses are nearly constant across P_{IN}. η_C falls below 50 µW because $E_{C(DC)}$ and $E_{C(TRAN)}$ do not scale with frequency and dominate over E_{ESR}, $E_{SW(MIN)}$, and $E_{C(DUTY)}$. With losses fixed, fractional losses rise with decreasing P_{IN} below 50 µW. Nevertheless, η_C at 6 mA is 1.4% and 7% more efficient than at 5 and 10 mA as it presents the optimum peak current in Fig. 3.8.

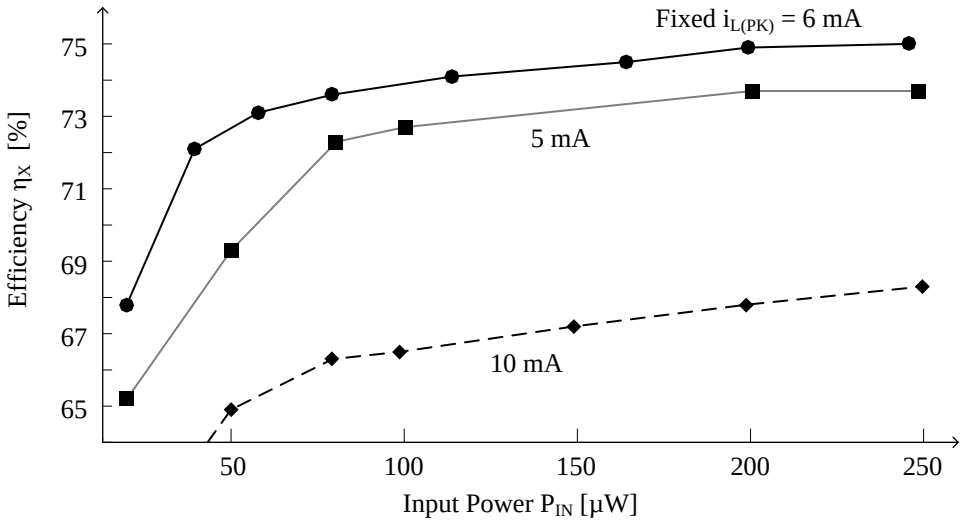


Fig. 3.12. Measured efficiency for fixed-peak and variable-frequency scheme.

3.2.5.3 Comparison

Figure 3.13 compares the power-conversion efficiencies η_X of both schemes for the 0.3-to-1.8-V boost 0.18-µm CMOS converter with a 47-µH–5.6-Ω inductor in discontinuous

conduction. With frequency fixed at 40, 80, and 120 kHz, η_C peaks at 57, 114, and 165 µW, at the power levels that correspond to the optimal $i_{L(PK)}$ and W_{SW} settings $i_{L(PK)}$' and W_{SW}'. In other words, $i_{L(PK)}$ and W_{SW} are optimal only at particular power levels. However the 6 mA fixed peak current scheme has universally high efficiency across the power range. In the photovoltaic scheme where the input power level can vary from few microwatts to 100 µW with the sensor movement from indoor condition the fixed packet variable frequency scheme is more suitable to reduce losses and transfer efficiently.

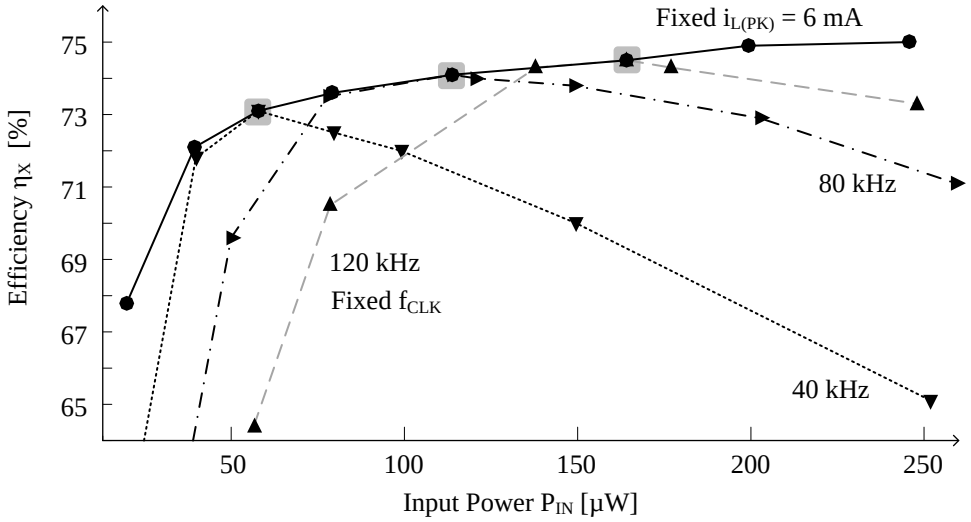


Fig. 3.13. Measured efficiency for fixed-peak and fixed-frequency schemes.

3.2.6 Comparison with Switched-Capacitor

The state-of-art implements the SC and SI under different premises of P_{PV} range and converter size. To compare the performance of SI and SC circuit [47] the following premises are set in a 0.6µm CMOS technology with a microwatt controller [38], C_{IN} is the PV cell's inherent capacitance (roughly 1nF), $v_{PV(OPT)}$ is 0.55V with a maximum allowed ripple of 50 mV across it, and a 1-V super capacitor acts as the battery. SI circuit

uses a chip size 220-µH inductor. The maximum ripple across v_{PV} restricts C_{FLY} size to 550 pF. The ohmic losses and gate drive losses scale for both the converters scale with P_{PV} in Fig. 3.14.

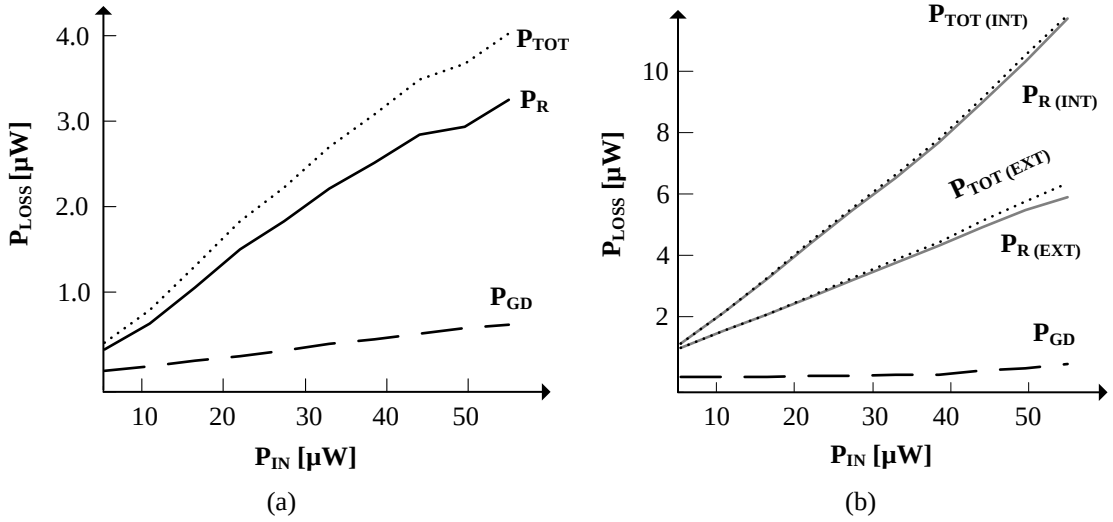


Fig. 3.14. Power stage losses (a) switched-inductor (b) switched-capacitor.

P_R is lower in SI converters, however, because for the same P_{PV}, i_L's peak is lower than i_{CFLY}'s in SC circuits, which means RMS currents are higher in SC implementations. P_R is considerably higher for on-chip implementations due to the bottom-plate capacitance loss. In other words, SC circuits trade efficiency for integration. SI converters can boost to any voltage using the two-switch topology, however the SC needs more capacitors and switches that suffer efficiency losses to boost to higher voltages. Additionally, the efficiency of the SC circuits degrades with deviation from the quantized boosting value [105]. This is particularly important as battery voltages spans for example 0.9 – 1.6 V for NiCd's, and, 2.7 – 4.2 V for Li Ions. In other words, SI circuits that use only one chip-size inductor seems a better choice for a PV harvesting system.

3.3 Switched-Inductor Charger–Supplies

The charger-supply circuits performs the twin functions of charging a battery and supplying the load. In the context of photovoltaic harvesting micro sensors, the sensor presents the load, the photovoltaic cell is the source and an electrochemical battery or capacitor allows for temporary energy store. The switched inductor power supplies relies on an external bulky inductor to transfer energy [109]–[117]. Using separate inductor power stages to implement the charging and supply functions [113] is unattractive dues to its large volume. Fortunately single-inductor multiple input multiple output power stages can implement both charging and supply function with a single power stage that restricts the use of inductors to just one. Among the single inductor PV charger-supply power stages, some transfers charge to the battery first and then supply the output and some supplies the output and from the output charge the battery [111], [119]. In both these case there is double efficiency hit transferring power through the inductor twice to reach the eventual destination. Other topologies that transfer energy from a single PV cell to battery and load with a single step and as a result efficient transfer can broadly classify to non-reversing and reversing topologies. In the non-reversing topology inductor current flow is unidirectional and in the reversing case it is bidirectional.

3.3.1 Topology

3.3.1.1 Non-Reversing

The non-reversing inductor L_X in Fig. 3.15 [113]–[116] steers power in one direction only. To derive and supply power from v_{PV} and v_{BAT} to v_O and v_{BAT}, switches S_{PV} and $S_{B(AID)}$ connect the receiving terminal of L_X at v_{SW1} to v_{PV} and v_{BAT} and S_O and $S_{B(CHG)}$

connect the supply terminal at v_{SW2} to v_O and v_{BAT}. This way, and with ground switches S_{G1} and S_{G2}, S_{PV}–S_{G2} energize L_X from v_{PV} and S_{G1}–S_O drain L_X into v_O and S_{G1}–$S_{B(CHG)}$ into v_{BAT}. Similarly, $S_{B(AID)}$–S_{G2} energize L_X from v_{BAT} and S_{G1}–S_O drain L_X into v_O.

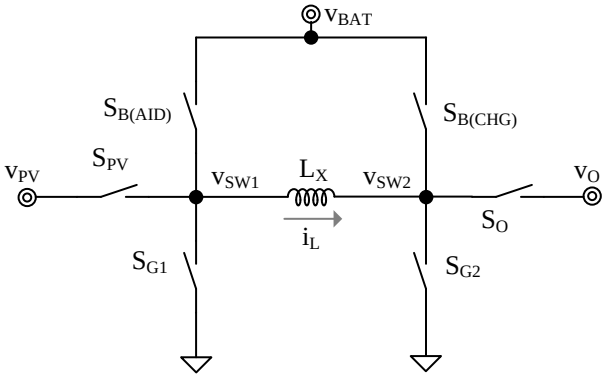


Fig. 3.15. Non-reversing switched-inductor charger–supply.

3.3.1.2 Reversing

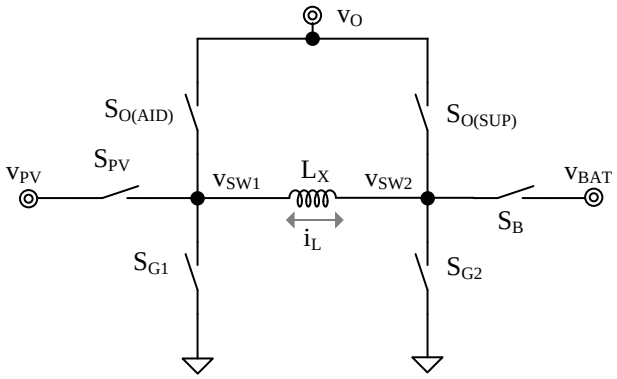


Fig. 3.16. Reversing switched-inductor charger–supply.

The reversing inductor L_X in Fig. 3.16 [104]–[111] conducts in both directions. L_X steers PV power P_{PV} to the right to v_O and v_{BAT} and battery-assistance power $P_{B(AID)}$ to the left to v_O. So S_{PV}, $S_{O(SUP)}$, and S_B connect L_X from v_{PV} to v_O and v_B and S_B and $S_{O(AID)}$ from v_{BAT} to v_O. This way, and with ground switches S_{G1} and S_{G2}, S_{PV}–S_{G2} energize L_X from

v_{PV} and S_{G1}–$S_{O(SUP)}$ drain L_X into v_O and S_{G1}–S_B into v_{BAT}. Similarly, S_B–S_{G1} energize L_X from v_{BAT} and S_{G2}–$S_{O(AID)}$ drain L_X into v_O.

3.3.2 CMOS Charger–Supplies

The most important difference between switched inductors in Section 3.3.1 is voltage swing because capacitances require more gate-drive power to charge across higher voltages. Although v_{SW2} in both networks swings to v_O and v_{BAT}, v_{SW1} in the non-reversing inductor of Fig. 3.15 swings to v_{PV} and v_{BAT} and in the reversing case of Fig. 3.16 to v_{PV} and v_O. So when v_{PV} is less than v_O and v_{BAT}, which is often the case [59], and v_O is greater than v_{BAT}, the non-reversing scheme swings and consumes less than the reversing counterpart, and *vice versa*. This means, the non-reversing topology is more efficient when L_X boosts v_{PV} and v_{BAT} to v_O and the reversing inductor is more efficient when L_X boosts v_{PV} and bucks v_{BAT} to v_O. This is why simulated losses in Fig. 3.17 are increasingly higher for the non-reversing case when v_{BAT} climbs above v_O's 1 V to 1.8 V.

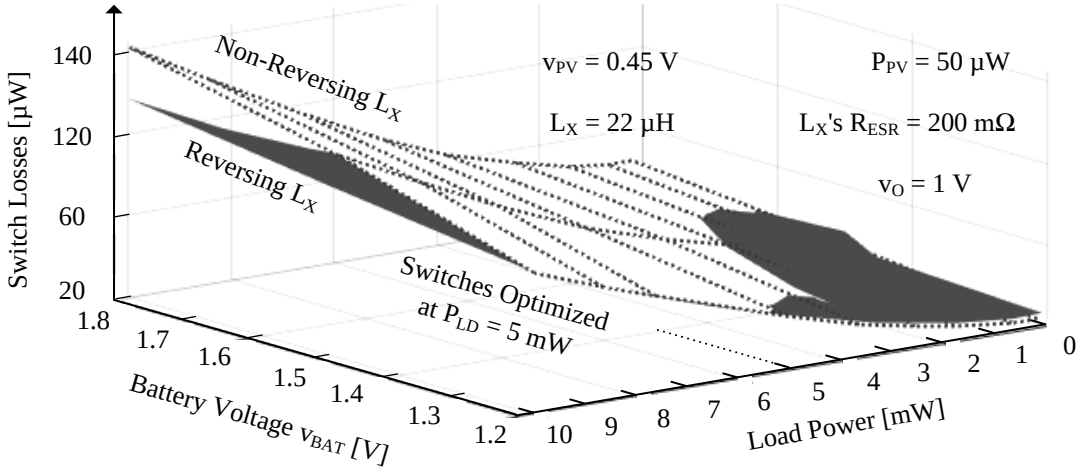


Fig. 3.17. Simulated switch losses for reversing and non-reversing inductors.

3.3.2.1 Boost-Boost Configuration

3.3.2.1.1 Headroom

Since stacked PV cells lose space and mismatch power between cells [56], v_{PV} is usually one PV cell at 0.4–0.5 V. v_O is usually so high in boost–boost applications that v_O-gated NFETs at v_{PV} in Fig. 2 offer much less resistance and capacitance than ground-gated PFETs. This is why S_{PV} is an NFET M_{PV} in the boost–boost charger–supply of Fig. 3.18.

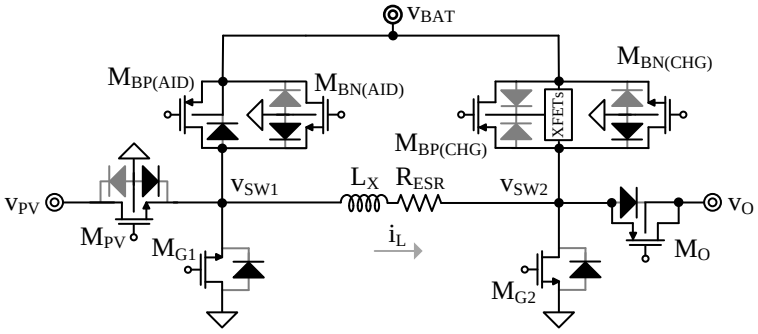


Fig. 3.18. Boost–boost switched-inductor CMOS charger–supply.

When v_O is the highest voltage, v_O-gate NFETs at v_O are ineffectual, so S_O in Fig. 3.15 is a PFET M_O in Fig. 3.18 with its bulk at v_O. Similarly, ground switches are NFETs M_{G1} and M_{G2} because ground-gate PFETs cannot close. Since v_{BAT} can be between v_{PV} and v_O in boost–boost cases, v_{BAT} switches $S_{B(AID)}$ and $S_{B(CHG)}$ can include both NFETs and PFETs.

3.3.2.1.2 Dead-Time Paths

The circuit should conduct L_X's current i_L across dead-time periods t_{DT} to the highest and lowest potentials available. Fortunately, NFETs at v_{SW1} incorporate grounded body diodes that can feed L_X across t_{DT}. Since v_O is the highest potential in boost–boost

applications, v_O's M_O incorporates a body diode that can similarly steer i_L to v_O. $M_{BP(CHG)}$'s body diode to v_{BAT}, however, should not conduct. This is why cross-coupled FETs block $M_{BP(CHG)}$'s diodes.

Although i_L should always flow to the right, the controller might inadvertently allow i_L to reverse. Connecting $M_{BP(AID)}$'s bulk to v_{BAT} both eliminates its bulk effect and introduces a body diode that can steer reverse i_L to v_{BAT}. NFETs at v_{SW2} incorporate grounded diodes that can similarly feed L_X when i_L reverses.

3.3.2.2 Boost-Buck Configuration

3.3.2.2.1 Headroom

Since v_{BAT} is higher than v_O in boost–buck applications, L_X in Fig. 3.16 can energize directly into v_O. That means, S_B and $S_{O(AID)}$ can energize L_X, instead of S_B and S_{G1}. S_{G1} is therefore unnecessary in Fig. 3.19. And v_{PV} is so low [59] and v_{BAT} so high that v_{BAT}-gated NFETs at v_{SW1} offer much less resistance and capacitance than ground-gated PFETs, so S_{PV} is an NFET M_{PV}.

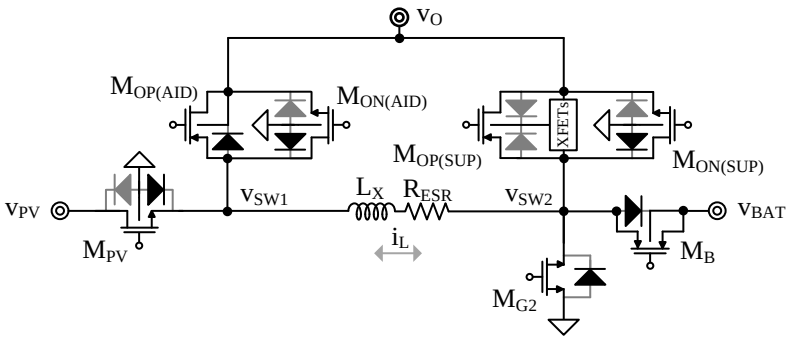


Fig. 3.19. Boost–buck switched-inductor CMOS charger–supply.

With no voltage higher than v_{BAT}, v_{BAT}-gate NFETs at v_{BAT} are ineffectual, so S_B is a PFET M_B with its bulk at v_{BAT}. Ground switch S_{G2} is an NFET M_{G2} because ground-gate PFETs cannot close. v_O switches $S_{O(AID)}$ and $S_{O(SUP)}$, however, can incorporate NFETs and PFETs because v_O can be anywhere between v_{PV} and v_{BAT}.

3.3.2.2.2 Dead-Time Paths

The circuit should conduct i_L across dead-time periods t_{DT} to the highest and lowest potentials available. NFETs at v_{SW1} incorporate grounded body diodes that can feed i_L and PFET $M_{OP(AID)}$'s diode can sink i_L into v_O, the highest potential at v_{SW1}. NFET diodes at v_{SW2} can similarly feed i_L and PFET M_B's diode sink i_L into v_{BAT}, the highest potential at v_{SW2}. $M_{OP(SUP)}$'s diode to v_O at v_{SW2} should not conduct, so cross-coupled FETs block $M_{OP(SUP)}$'s diodes.

3.3.3 Design Variations

3.3.3.1 Asynchronous simplifications

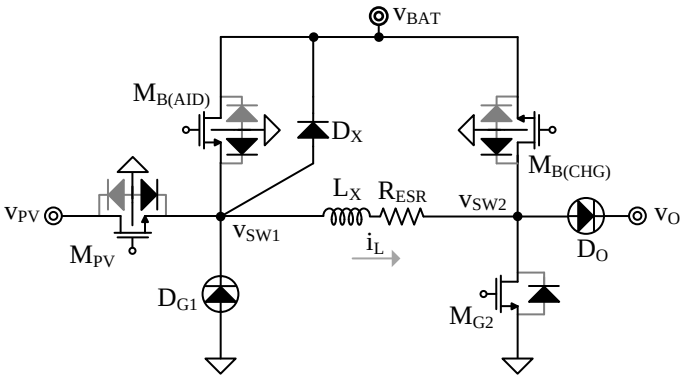


Fig. 3.20. Simplified boost–boost switched-inductor CMOS charger–supply.

Non-reversing switches that conduct dead-time currents in the same direction can be diodes. Ground and v_O FETs M_{G1} and M_O in the boost–boost of Fig. 3.18 and v_O FETs in the boost–buck of Fig. 3.19 $M_{OP(AID)}$ and $M_{ON(AID)}$, for example, conduct i_L in and out of dead time in one direction. So diode or diode equivalents can replace them like Figs. 3.20 and 3.21 show.

3.3.3.2 Gate-drive simplifications

If v_{BAT} is low and well below v_O in the boost–boost of Fig. 3.18, v_{BAT}'s ground-gate PFETs $M_{BP(AID)}$ and $M_{BP(CHG)}$ can be much more resistive than v_O-gate NFETs. So removing these PFETs like Fig. 3.20 shows can be as efficient with less area. Without v_{SW1}'s $M_{BP(AID)}$, however, reverse i_L has no path, so adding a protection diode D_X to v_{BAT} in Fig. 3.20 is prudent.

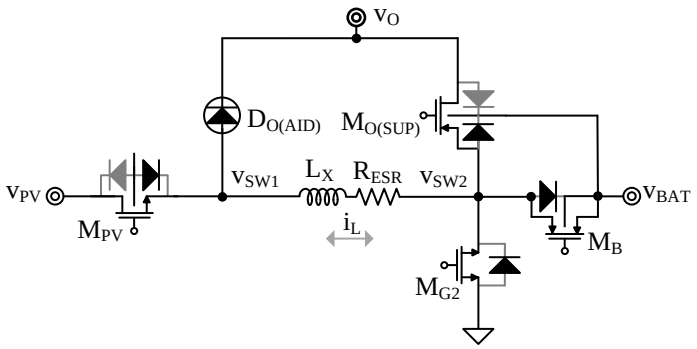


Fig. 3.21. Simplified boost–buck switched-inductor CMOS charger–supply.

v_O's v_{BAT}-gate NFETs in the boost–buck of Fig. 3.19 can similarly lose more power than ground-gate PFETs when v_{BAT} falls towards v_O, like Fig. 3.22 shows. So if v_O is high and close to v_{BAT}, removing v_O NFETs $M_{ON(AID)}$ and $M_{ON(SUP)}$ like Fig. 3.21

shows can be as efficient with less area. And if close enough to v_{BAT}, bulk effect in v_O PFET $M_{O(SUP)}$ from connecting its bulk to v_{BAT} might not be significant.

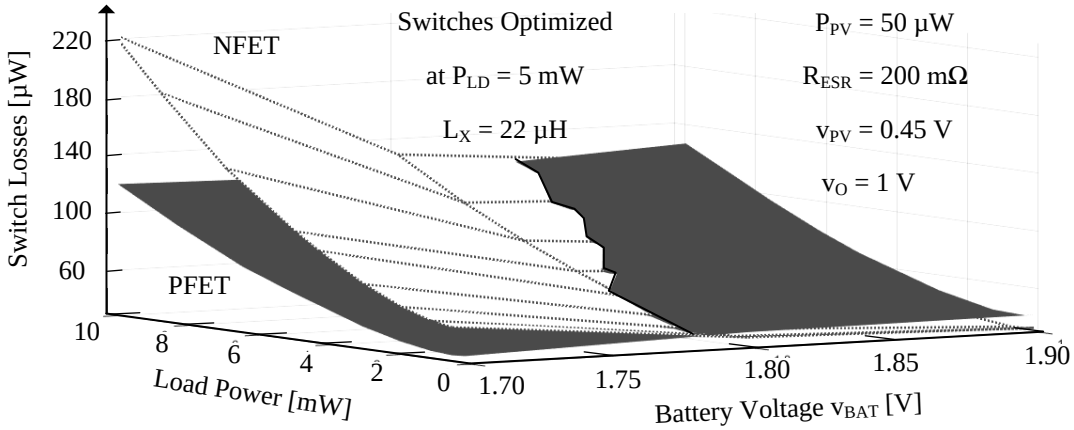


Fig. 3.22. Simulated NFET and PFET losses in $S_{O(AID)}$ from the boost–buck.

3.3.3.3 Inductor ESR considerations

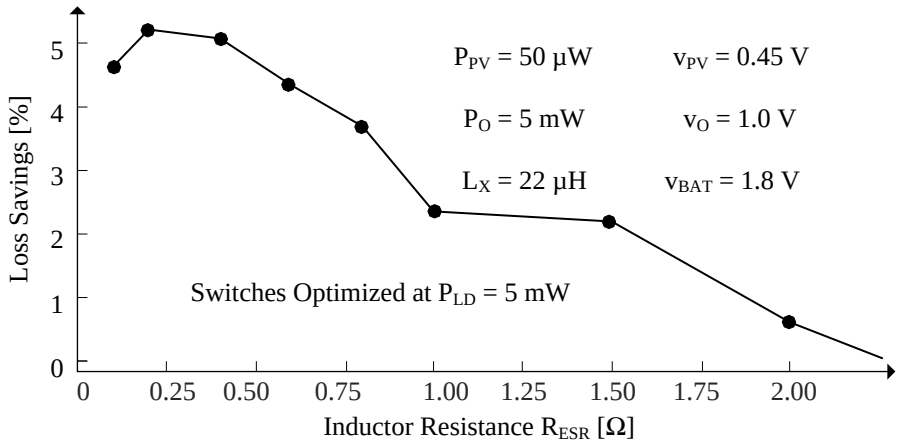


Fig. 3.23. Simulated loss savings of the reversing over non-reversing schemes.

High-inductance L_X, low-resistance R_{ESR} inductors transfer lots of power with little losses. More turns and thicker coils, however, require more space. So, tiny inductors burn more power with higher L_X. And as R_{ESR} losses in P_{ESR} climb, switch losses P_{SW} are less significant Fig. 3.23. As a result, the loss savings of a low-loss network diminish with

higher R_{ESR}. So although the reversing scheme in Fig. 3.16 is up to 5% more efficient with low R_{ESR} in Fig. 3.23, the non-reversing case in Fig. 3.15 [110] is nearly as efficient above 2.2 Ω.

Since switch losses lose significance with high R_{ESR}, silicon area becomes more important. So instead of using low-loss channel widths, which balance ohmic and gate-drive losses [117], switches can be narrower, and therefore, smaller. The fractional switch losses are greater than 10% for R_{ESR} less than 2.2 Ω. Above this resistance by keeping fractional switch losses at 10% by reducing the switch size. The switches in the reversing circuit of Fig. 3.16 occupy up to 20000 μm^2 or 80% less silicon area when R_{ESR} is greater than 5.5 Ω, as Fig. 3.24 demonstrates.

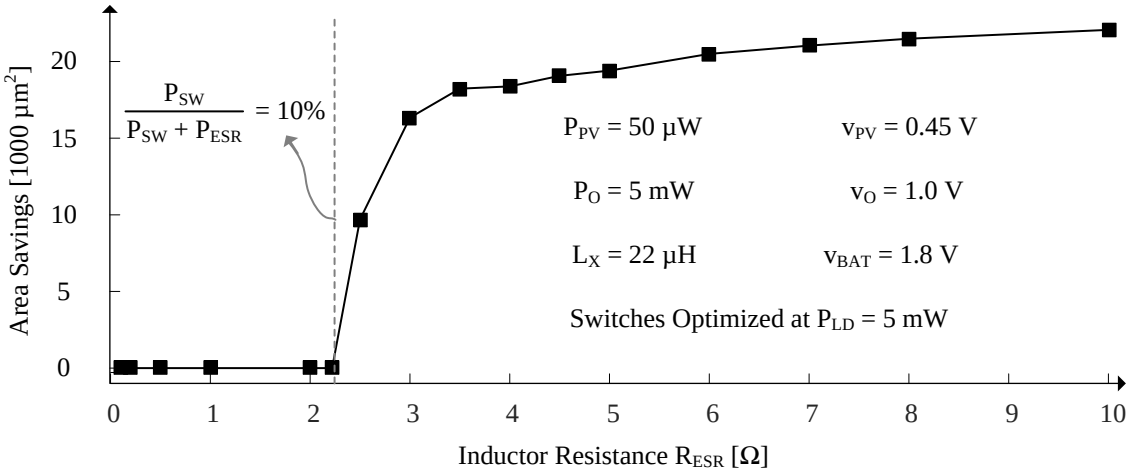


Fig. 3.24. Simulated area savings of the reversing over non-reversing schemes.

3.4 Summary

To maximize harvested output power, the circuit should be efficient, which is to say it should transfer and condition power by switching an in-package inductor. Still, Ohmic losses P_R are dominant and proportional to P_{PV}, with controller quiescent power P_Q not

far behind and gate-charging losses P_G further back. Interestingly, capacitor-based circuits consume more power because they conduct higher RMS currents. Moreover, on-chip implementations lose additional power in charging and discharging parasitic bottom-plate capacitors. In other words, switched-inductor harvesters harness more light energy from chip-sized PV cells than switched-capacitor circuits, which is especially important when P_{PV} is low, cloud cover and artificial lighting conditions persist, and unobtrusiveness (i.e., integration) is imperative. This chapter shows how to design low-loss battery-assisted photovoltaic-sourced CMOS charger–supplies. And that non-reversing switched inductors are less lossy than the reversing counterparts when the output voltage is greater than the battery voltage, and *vice versa* otherwise. Headroom, dead-time currents, and reverse-current protection dictate which and how FETs should switch the network. Unidirectional switches that conduct dead-time currents in the same direction can be diodes or diode-emulating FETs. But as inductor resistance and losses climb, the benefits of low-loss CMOS choices diminish. In these cases, switches can be more lossy, and as such, occupy up to 80% less silicon area.

CHAPTER 4. FEEDBACK CONTROLLER

The feedback controllers primarily function is to regulate the output supply voltage tightly and robustly about a reference voltage while supplying power efficiently [105]–[115]. The output voltage ripples about the reference across the load range and in response to load dumps are key performance parameters for the feedback control [105]. This research implements two partially different control schemes for the reversing and non-reversing power stages in Chapter 3. The rest of the chapter presents the control method, for the two prototypes reversing and non-reversing that this research implements, in light of different lighting and load conditions for both the reversing and non-reversing circuits.

4.1 Power Flow

In the context switched-inductor power transfer circuits, to transfer power between a source and load that operate at different voltages, the circuit energizes and drains L_X in the alternate phases of the switching cycle. There are two traditional mode of conduction for switched-inductor circuits are continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In DCM the circuit raises inductor current i_L to a peak value $i_{L(PK)}$ and drains it to zero allowing the system to switch at a lower frequency and at same time maintains the direction of current flow in the intended direction, thereby resulting in lower losses as [117] Chapter 3 shows. As a result in this research DCM is the preferred mode of operation and the flow of energy packets between source and load, and the frequency of transfer defines the power flow.

The charger–supply systems have the twin function of a providing a robust regulated voltage as well as charging the battery when excess harvested energy is available. In charger–supply systems, there are two modes of operation depending on where photovoltaic power P_{PV} is greater or lower than the load requirement P_{LD}. When heavily sourced the photovoltaic power exceeds the load P_{LD} at output v_O, in this case the excess power P_{CH} after satisfying the output can charge the battery v_{BAT}. However when load is heavy the photovoltaic power itself cannot satisfy the load requirement, in this case the system draws assistance from battery P_{SUP} to satisfy the excess load requirement past P_{PV} and losses. Across an average battery charge/discharge cycle the battery after losing some of the energy across the circuit can only provide slightly lower energy than what the system charges it with, therefore the duty cycle of the heavily sourced and battery assisted modes sets the supply lifetime of the system.

4.1.1 Heavily Sourced

In cases where the incident light level is quite high, for example in outdoor lighting conditions or even in moderate lighting conditions with the load at a low value (when the system is idling), the photovoltaic power that the PV cell v_{PV} provides can be greater than P_{LD} at v_O. When PV power exceeds P_{LD}, the mode is heavily-sourced, as the photovoltaic source is heavier in comparison with the load requirement. In this mode the system stores the excess power after satisfying the load by charging the battery. Since the circuits operates in DCM the size, direction and frequency of transfer packets of energy dictates power flow. As Fig. 3.13 shows to maximize efficiency of transfer the packet size is fixed.

To draw maximum power from PV cell the system adjust the frequency of energy packets E_{PV} that it draws from the PV cell depending on the light level. In case the load requires energy, the systems de-energizes the energy packet to v_O as Fig. 4.1 shows However since P_{PV} is larger than P_{LD} successive E_{PV} packets charge the output capacitor at v_O more than the load current i_{LD} discharges. As a result the successive energy packets E_{PV} satisfies the output, after which the system steers the next several few packets to battery, Fig. 4.1., and charge it until the output requires power again.

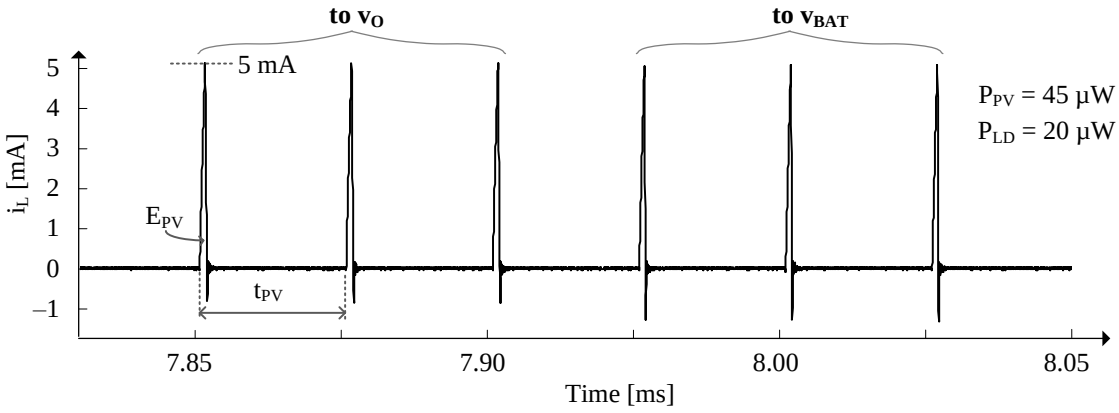


Fig. 4.1. Measured inductor current waveforms in HS mode for non-reversing power stage.

In Fig. 4.1 with the P_{PV} of 45 µW and P_{LD} of 20 µW the non-reversing power stage, Fig. 3.15., that employs a 47 µH inductor draws 5mA peak current E_{PV} packets are drawn every 25 µs, or f_{PV} of 40 KHz. It delivers 80 energy successive energy packets to the output and follows it with 100 charging packets to the battery every output cycle. In this mode the power flow in case of a reversing power stage of Fig. 3.16 is similar as Fig. 4.2. The peak energy packet size is larger at 11 mA in this as the system employs a 22 µH inductor, the number of successive energy packets are higher around 500 as the systems also employs a larger output capacitor of 10µF.

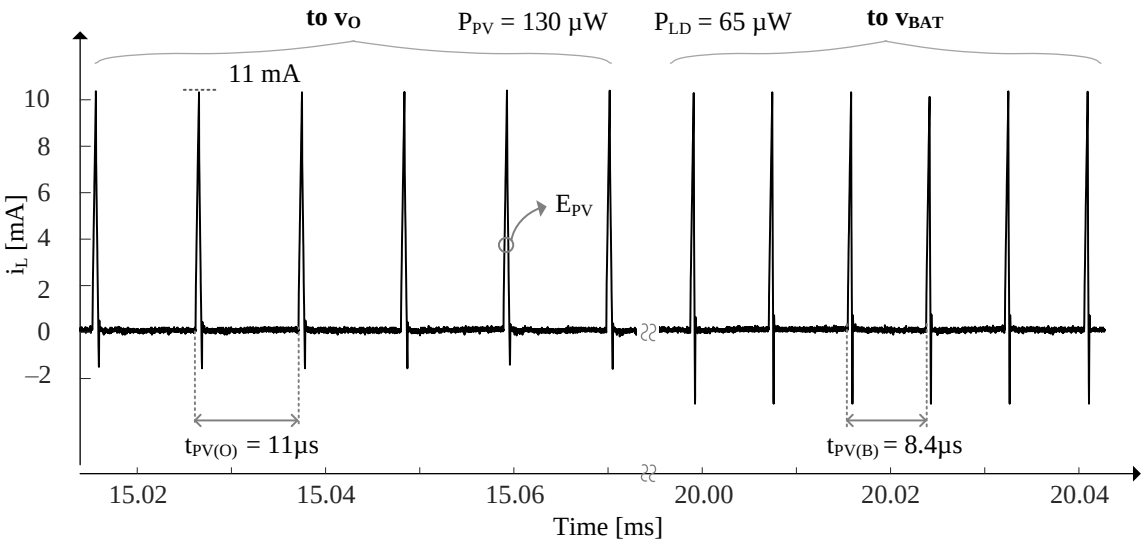


Fig. 4.2. Measured inductor current waveforms in HS mode for reversing power stage.

4.1.2 Battery-Assisted

In cases where the system is in indoors lighting conditions and the sensor load is non-idling or during transmission and reception events even in outdoor lighting condition the sensor power overwhelms P_{PV}. For example the during a transmission event the sensor can draw upto 10 mW power, however the maximum P_{PV} even in sunlight is less than 150 µW. Therefore in the battery-assisted mode the battery provides the excess power the load requires beyond what PV cell can provide. Since the P_{PV} and P_{LD} are independent the battery-assistance is variable depending on the incident light and sensor operation. In DCM there are two possible methods to transfer variable power levels either varying the size of a single- energy packet (variable-packet) or sending variable number of fixed size packets within a clock period set by the PV packets.

4.1.2.1 Variable-Packet

When load P_{LD} demands more than PV cell's power P_{PV}, v_{BAT} supplies the remaining power. So, every clock cycle t_{PV}, the PV cells sends an energy packet E_{PV} and battery follows it with the battery packet E_{BAT}. To send E_{PV} L_X's i_L rises to 5 mA and falls to zero to deliver the equivalent of 40 µW across 25 µs to v_O. For sending the battery packet i_L rises to 17 mA across t_{BE} in Fig. 4.3 and falls to zero to deliver to v_O the remaining 960 µW that the 1-mW load requires. Here the system in every photovoltaic cycle t_{PV} delivers only one photovoltaic packet and one battery packet to v_O to satisfy it. As the output load rises or falls the system regulates the battery packet size to rise or fall proportionally. The conduction losses scale quadratically with the inductor peak current and load power scales linearly as a result the efficiency of transfer drops at higher power. However the PV packet size, direction and frequency remains constant in response to the load changes and depends only on the light level. In the system implements a constraint of minimum battery packet size of 1 mA to maintain logic integrity and maximum peak current of 30 mA for protection.

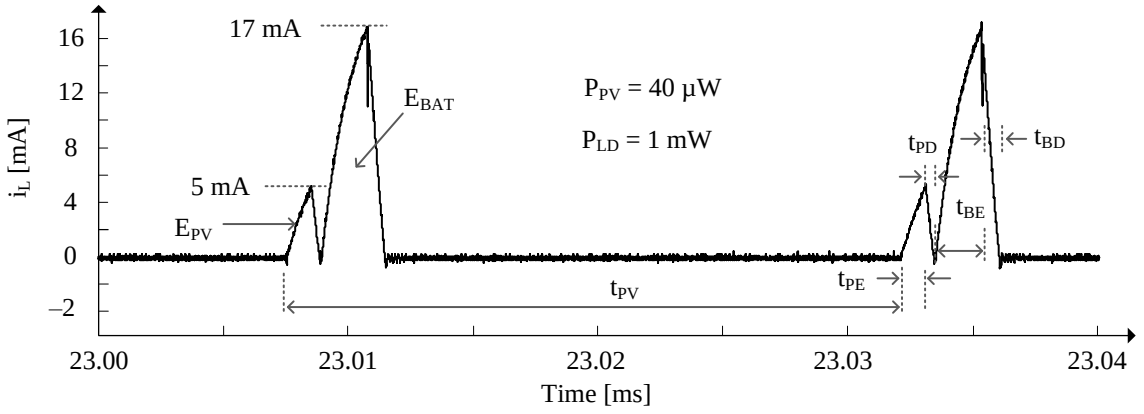


Fig. 4.3. Measured BA mode variable packet inductor current in non-reversing circuit.

4.1.2.2 Multiple Packets

To address the challenge of low efficiency at higher power levels the controller can send multiple optimized-size energy packets from the battery instead of a single variable size one as Fig. 4.3 shows. Since each constant size energy packet represents a fixed energy content and associated conduction and gate-drive losses, sending multiple of them scales the power the system delivers with the loss it incurs proportionally and the efficiency holds steady. In this control schemes as well the system delivers one packet from the photovoltaic cell at the beginning of every clock cycle and but follows it with multiple equal size energy packets to satisfy the load. In Fig. 4.4 the reversing circuit, Fig. 3.16., the 11 mA peak current PV packet supplies 130 µW of power to the output and the successive battery packets supply the remaining 9.9 mW of the total 10 mW load requirement.

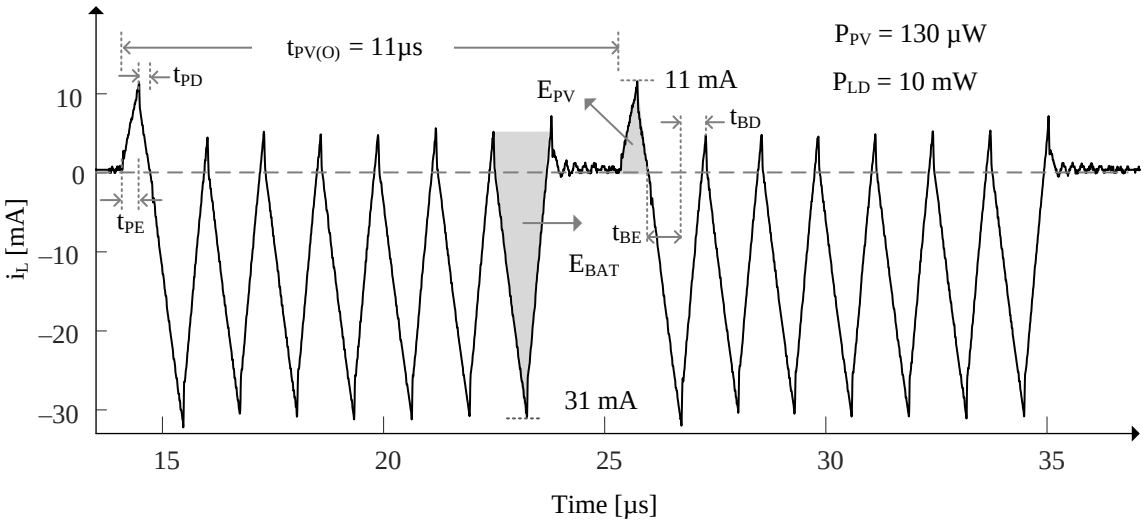


Fig. 4.4. Measured multiple packets inductor current waveforms in BA mode.

The reversing nature of the circuit causes inductor current to switch directions however in both cases the inductor delivers power to v_O and doesn't discharge it. Another

interesting aspect in this converter is the quantized nature of power transfer in each cycle. In response to load demand the controller delivers only zero or positive integer number of fixed size packets every cycle this way if the load requirement is not a multiple of the packet energy then the number packets switch between providing more power or less power each successive cycle so as to satisfy the output on average. The system also implements a blank time or period of no conduction before every PV packet to avoid overlap between packets. The number of packets in each cycle can be 0–70 packets at P_{PV} of 10 µW and 0–7 packets at P_{PV} of 130 µW.

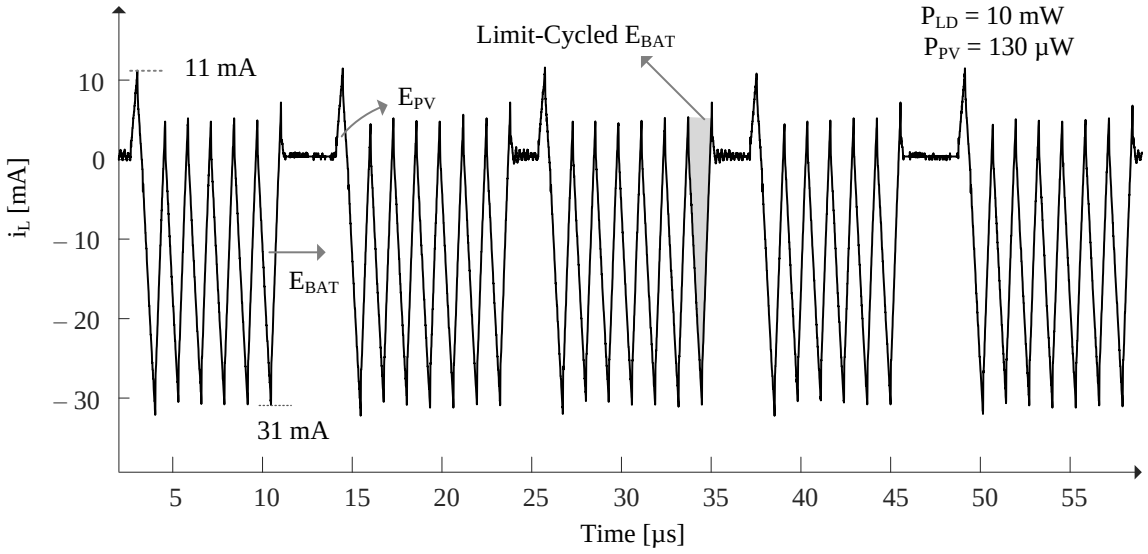


Fig. 4.5. Measured multiple packets inductor current limit-cycling in BA mode.

4.2 Heavily Sourced

In this mode of operation P_{PV} is greater than P_{LD} therefore the controller directs just enough number of energy packets from photovoltaic cell to the output v_O to satisfy it and redirects the rest to charge the battery. For this purpose the controller needs to have intelligence to evaluate whether the output is satisfied and deliver power to it otherwise.

Measuring the instantaneous load requirement by measuring load current is both costly and lossy. As a result [102], hysteretic control that just evaluates the load power indirectly by measuring output voltage is preferable, Fig 4.6.

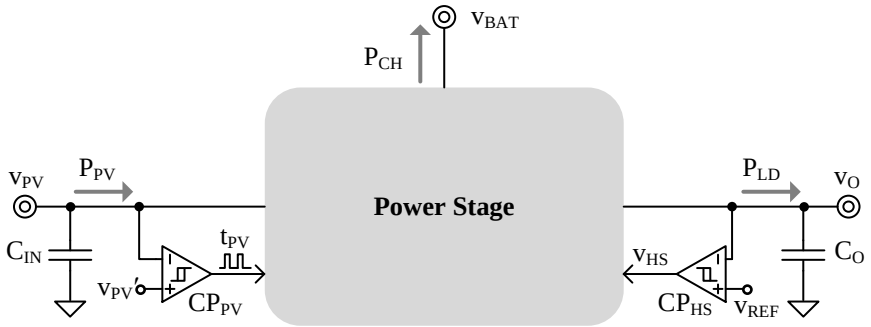


Fig. 4.6. Heavily sourced mode controller.

In this mode since P_{PV} is greater than P_{LD} the charge that a photovoltaic packet E_{PV} provides is always greater than the total charge the load current i_{LD} discharges from the output capacitor C_O at v_O every photovoltaic cycle. This sets a trend of output rising when successive E_{PV} packets reach C_O and when successive E_{PV}'s goes to the battery instead the load current unilaterally discharges C_O and v_O falls. In the hysteretic control a duty-cycled comparator CP_{HS}, Fig. 4.6, turns on during the energizing time of the PV packet and senses the output voltage v_O and compares it with a reference v_{REF}. If v_O is a threshold v_{HYS+} higher than the v_{REF} then the system concludes the output is satisfied and redirects the PV packets to battery and if v_O is a threshold below v_{REF} the system steers the packets to the output.

In the controller, comparator CP_{HS} measures the output and compares it with v_{REF} during the initial half of the energizing time of the PV packet and latches the decision at end of half the energizing time this way the comparator makes decision of the packet

direction before it delivers it. Another option is to measure the output continuously when the packet is de-energizing and switch the direction on the fly when the comparator output switches [102], thereby sharing packet this method can be appear slightly more accurate. However since the de-energizing time is in the order few 100 ns putting higher speed requirement on the comparator, also there is a finite dead time that system requires to turn off a switch and turn on another one during this time i_L flows through a diode and losses energy.

4.2.1 Output Ripple

The hysteretic comparator CP_{HS} compares the output voltage with a reference to decide the direction of power flow. In Fig 4.6, CP_{HS} continue to direct PV packets to the output until v_O goes V_{HYS+} above v_{REF} after which it redirects the packets to the battery and wait tills the load discharges v_O to V_{HYS-} below v_{REF} to again direct the packets to the output and the cycle continues. So the hysteretic controller behaves as an oscillator which regulates the ripple of the output voltage with a hysteretic window V_{HYS+} to V_{HYS-} about v_{REF} the variations in the hysteretic window of comparator due to mismatches in the circuit implementation can offset the average output voltage about the reference value.

Since the comparator is duty-cycled the photovoltaic period determines how often the decisions are made and long photovoltaic period can lead to output rising or falling few millivolts above or below the trip point before the decision is made. In both the non-reversing and reversing implementation the output capacitor at 2.2 µF and 10 µF are large enough that even in the longest target PV period of 100 µs the output doesn't exceed the trip point by 2 mV.

In the non-reversing system of Fig 3.15 the system energizes a 47 µH inductor to 5 mA peak current and steers packets to the 2.2 µF capacitor or the battery depending on the output voltage. When the systems steers the PV packets to the battery, v_O drops as P_{LD} discharges C_O until it hits a lower threshold 25 mV below v_{REF}, at 6.1 ms in Fig. 4.7, and CP_{HS} trips high. This triggers the system to steer all the PV packets to v_O. Since PV power is greater than P_{LD} in this mode v_O rises. When v_O rises 25 mV above v_{REF}, at 7.9 ms, CP_{HS} trips v_{HS} low and further directs the PV packets to recharges the battery, v_O starts decreasing at this point and hits the lower threshold at 10.4 ms and the process repeats. The offset of the CP_{HS} implementation is about 1 mV and as a result the lower hysteric window is slightly lower than the upper hysteretic window. At maximum 25 mV ripple about 1V reference the hysteretic control regulates the v_O to 2.5 % of the target value.

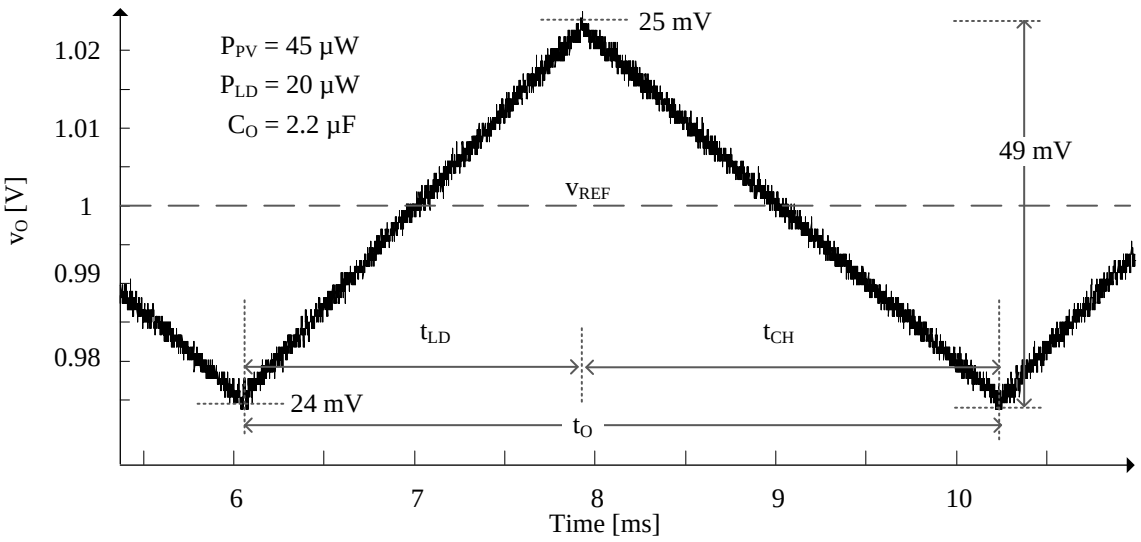


Fig. 4.7. Measured output when heavily sourced for non-reversing circuit.

In the reversing system of Fig 3.16 the system energizes a 22-µH inductor to 11 mA peak current and steers packets to the 10 µF capacitor or the battery depending on the

output voltage. When the systems steers the PV packets to the battery, v_O drops as P_{LD} discharges C_O until it hits a lower threshold 28 mV below v_{REF}, at 10.5 ms in Fig. 4.8, and CP_{HS} trips high. This triggers the system to steer all the PV packets to v_O. Since PV power is greater than P_{LD} in this mode v_O rises. When v_O rises 28 mV above v_{REF}, at 18 ms, CP_{HS} trips v_{HS} low and further directs the PV packets to recharges the battery, v_O starts decreasing at this point and hits the lower threshold at 24.5 ms and the process repeats. The offset of the CP_{HS} implementation is near zero and as a result the lower hysteric window and the upper hysteretic window align well. At maximum 28 mV ripple about 1V reference the hysteretic control regulates the v_O to 2.8 % of the target value.

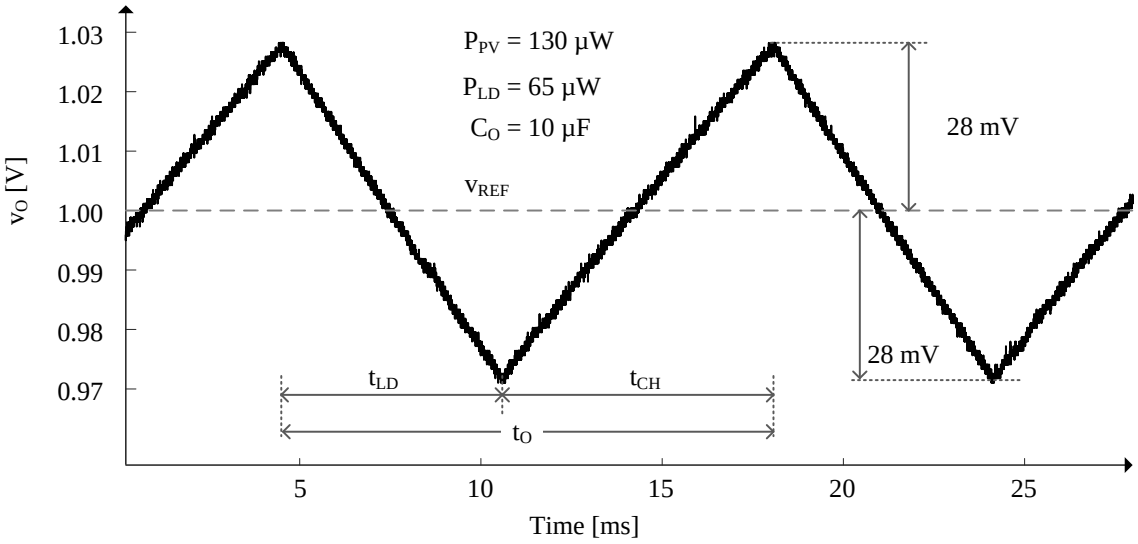


Fig. 4.8. Measured output when heavily sourced for reversing circuit.

4.2.2 Load Regulation

The hysteretic controller retains the upper and lower hysteretic thresholds across the load levels. However the time duration t_{LD} that output receives PV packets, the time duration the battery charges t_{CH} and the total period of the output voltage ripple, varies with the

load condition. For instance at constant incident light condition if the load power increases the proportion of PV packets that reaches output has to be greater than that reaching battery as battery receives only the excess energy after satisfying the load. Therefore t_{LD} dominates t_O when the load power is higher fraction of P_{PV} and t_{CH} dominates when P_{LD} proportion is lower. As a result, t_O rises with both lighter and heavier loads to produce the valley response shown in Fig 4.9.

The rate at which E_{PV} can charge the output depends on the load. Load also determines how soon the output discharges when the PV cell transfers its energy to the battery. For the non-reversing circuit at low P_{LD} around 10 µW, the 4.74-ms output discharging or battery charging time $t_{CHG,}$ occupies most of the 5.4-ms output voltage period t_O in Fig. 4.9. Similarly, when P_{LD} is high around 80 µ W, it is difficult or time consuming to charge the v_O, and the 8.5-ms output charging time t_{LD} dominates the 9.3-ms t_O. The minimum t_O of 2.3 ms or maximum output frequency f_O of 439 Hz occurs when P_{LD} is nearly half of P_{PV} as t_{CHG} equals t_{LD}.

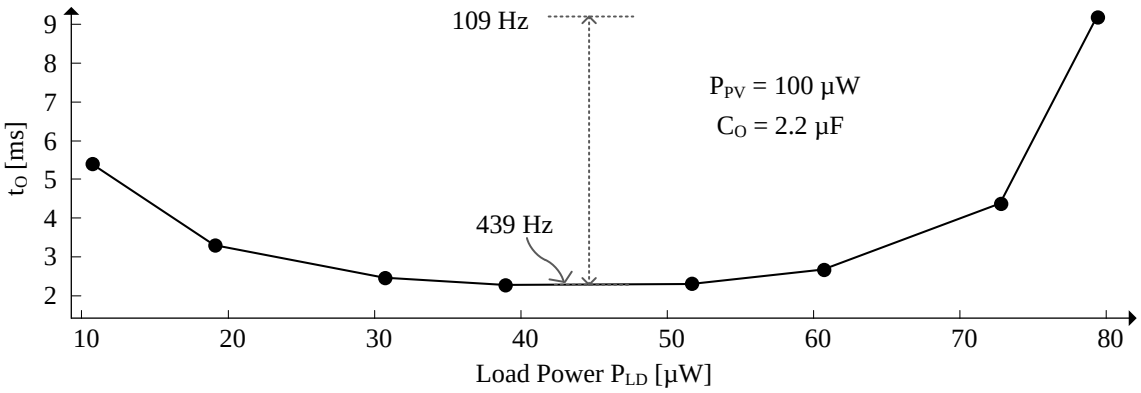


Fig. 4.9. Measured output period across load power when heavily sourced in a non-reversing circuit.

For the reversing circuit at low P_{LD} around 10 µW, the 26-ms output discharging or battery charging time $t_{CH,}$ occupies most of the 33-ms output voltage period t_O in Fig. 4.10. Similarly, when P_{LD} is high around 110 µ W, it is difficult or time consuming to charge the v_O, and the 60-ms output charging time t_{LD} dominates the 57-ms t_O. The minimum t_O of 9.4 ms or maximum output frequency f_O of 106 Hz occurs when P_{LD} is nearly half of P_{PV} as t_{CHG} equals t_{LD}.

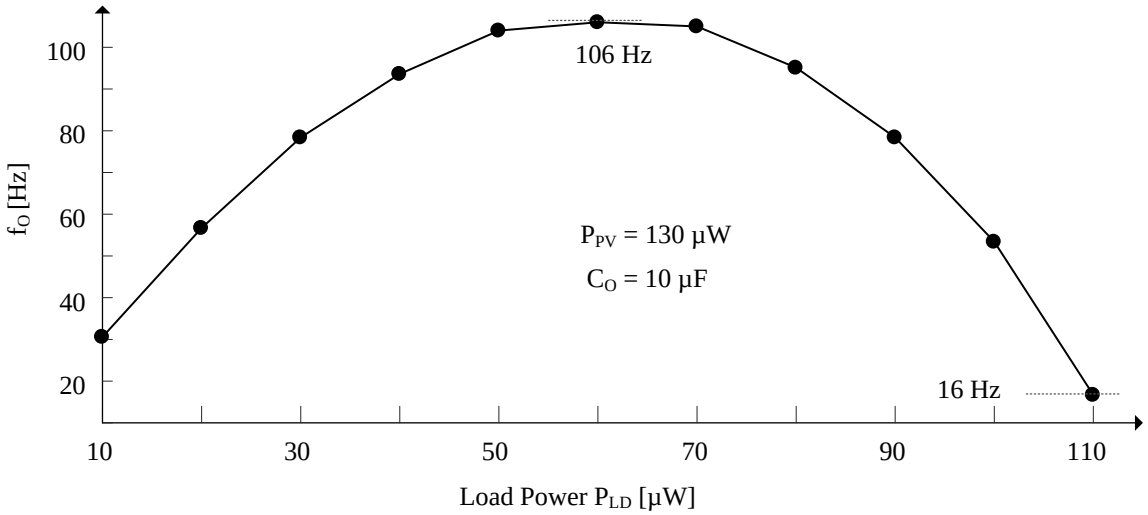


Fig. 4.10. Measured output period across load power when heavily sourced in a reversing circuit.

4.2.3 Battery-Charging

The controller diverts packets of energy to the battery when output cross the positive trip point. The power that system delivers to the battery depends on the difference between P_{PV} and P_{LD} as wells as the losses that the transfer of power incurs. Since the battery also supplies the controller at the battery voltage while charging rises only if system delivers it more power than what it draws from it. The charging rate across time therefore depends on the current reaching the battery after suppling the system as well on the size of the

battery itself. In case of a capacitor implementing the battery the voltage across the capacitor and its capacitance C_{BAT} is the measure of the energy $0.5C_{BAT}v_{BAT}^2$ it stores.

For the non-reversing circuit the battery in fig 4.11 only receives 60 µW of the 100 µW P_{PV} after satisfying a 20 µW load. In the Fig. 4.10, a 2×1.2×1-mm^3 10-µF capacitor implements the battery. The battery voltage across a 10 µF capacitor rises by 400 mV in less than 70 ms.

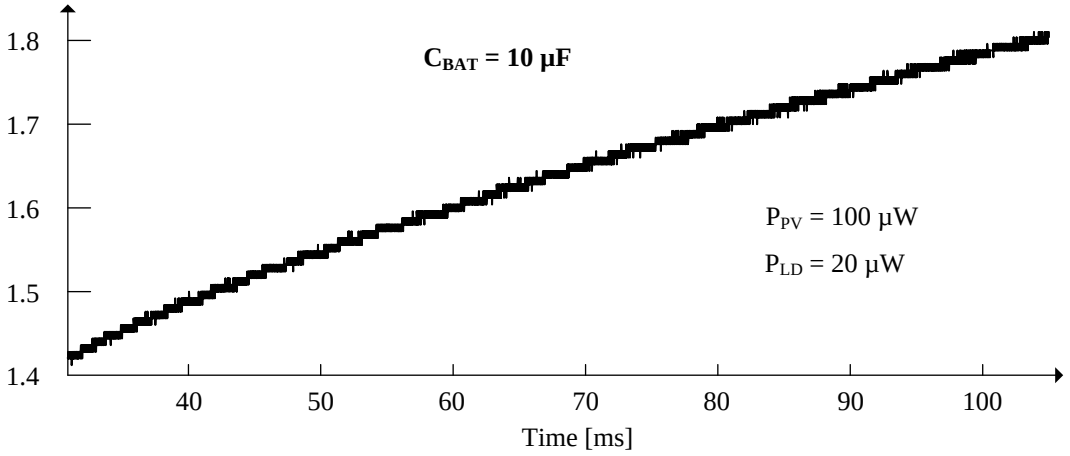


Fig. 4.11. Measured battery charging performance for a non-reversing circuit.

For the reversing circuit the battery in Fig 4.12 receives 70 µW of the 100 µW P_{PV} after satisfying a 20 µW load. In the Fig. 4.12, a 5×3.6×1.5-mm^3 14-mF super-capacitor implements the battery. The battery voltage across a 14 mF capacitor rises by 400 mV in less than 150 s. The larger size super capacitor takes longer time to charge but also stores higher amount of energy. Comparison with electro chemical batteries super capacitors offer the advantage of longer number of charging cycles and suits well with the intermittent charging profile of the controller.

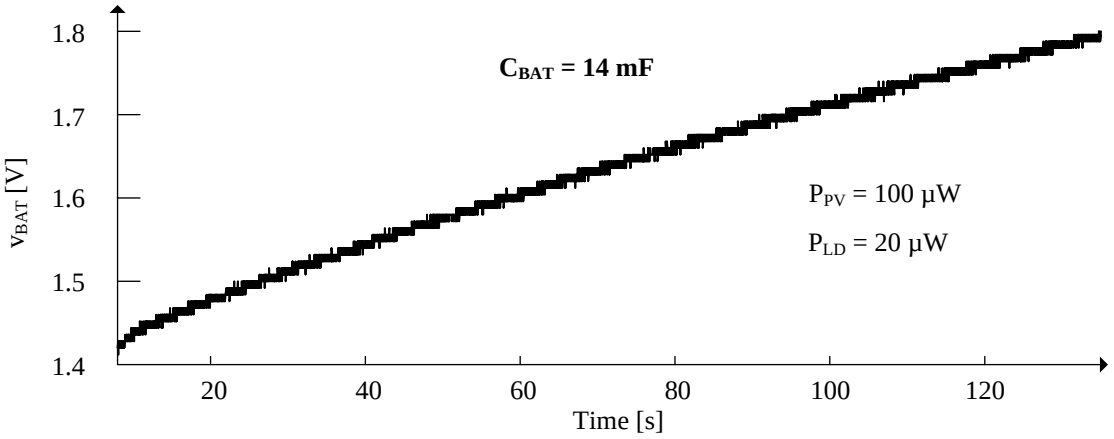


Fig. 4.12. Measured battery-charging performance for a reversing circuit.

4.2.4 Stability

The hysteretic controller employ negative sample the output voltage compares with reference and adjusts the switching sequence to dictates the direction of power flow. Since the comparator decides the direction of power flow faster than the system draws power from the PV cell as a result the over or undershoot of the output voltage is only by the margin of a single packet. The energy storage elements in the feedback path can retain and accumulate perturbations in energy levels across switching cycles to create large changes or oscillations in the circuit. In small signal terms the poles and zeros in the system sets the change in magnitude and phase of the loop gain and in cases where the phase drops to 180 degree before the loop gain falls below 1 the system has positive instead of negative feedback and the output voltage can grow and oscillate beyond the regulated margins. In the switched-inductor converters the inductor L_X and capacitor C_O introduces two such poles [38] and [118].

The circuit operates in DCM or in other words in every cycle the inductor current rises from and falls back to zero values. This means any perturbation in the inductor

current doesn't carry forward to the next cycle or in other words the inductor pole is absent in DCM. Also since any increase in energizing time also leads to a corresponding increase in de-energizing time to reset the current the out phase zero is also absent in DCM [38] and [118]. Therefore in DCM output capacitor C_O presents the dominant pole in the system:

$$p_O = \frac{1}{2\pi(R_O \parallel R_L)C_O}. \tag{4.1}$$

Where R_O represents the load resistance and R_L represents the equivalent resistance the inductor presents at the output. In fig 4.12 (a) a small signal circuit models the output impedance circuit that the transfer circuit presents the inductor connects to the output to the output only for the duration of the PV packet de-energizing time t_{PD}. A test voltage v_t can ramp the inductor current i_t in this duration to a peak value $i_{T(PK)}$. The ratio of the average test voltage v_t and average test current $i_{t(avg)}$ defines the inductor resistance:

$$R_L = \frac{v_{T(AVG)}}{i_{T(AVG)}} = \frac{v_T t_{PV}}{q_T} = \frac{v_T t_{PV}}{0.5 i_{T(PK)} t_{PD}} = \frac{v_T t_{PV}}{t_{PD}}\left(\frac{L_X}{0.5 v_T t_{PD}}\right) = \frac{2L_X t_{PV}}{t_{PD}^2} \tag{4.2}$$

Where q_t is the total charge in every cycle as Fig. 4.12 (b) shows.

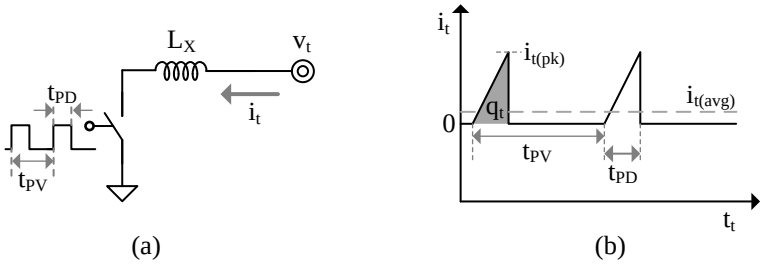


Fig. 4.13. DCM HS mode small signal output impedance (a) circuit (b) current.

So C_O introduces a pole p_O that C_O's low $R_{ESR.O}$ limits with an in-phase zero z_{ESR} at a frequency that is well above the system's bandwidth f_{0dB} [38]. The delay in the comparator also might introduce a pole but as the comparator delay is in the order of 10s of nano-seconds the pole is also decades above f_{0dB}. Since output pole solely decides the frequency response inside the systems bandwidth in this mode, the loop gain reaches f_{0dB} at –20 dB per decade with nearly 90° of phase margin, and the loop is stable.

4.3 Battery-Assisted

In the battery-assisted (BA) mode the photovoltaic cell cannot source sufficient power to meet the load requirement, in this case the energy in the battery can assist in meeting the load demand. But unlike the photovoltaic source the size and state of charge of the limits the energy it can supply so the system can engage in this mode only for few tens of milliseconds before the battery depletes. Also the amount of power the battery supplies can be as large as 10 mW and therefore efficiency is critical in this mode to extend the batteries supply lifetime. In this research the non-reversing and reversing power stages implement two different control schemes. In both cases the system still operates in DCM however in one case the battery delivers only a single variable size packet and in the other case the battery delivers multiple or variable number of fixed energy packets. As a result the efficiency, regulation, stability constraints are different between both control schemes and implementations.

4.3.1 Variable Packet

In battery-assisted mode, the P_{PV} is insufficient to supply P_{LD}, therefore output v_O receives a fixed energy packet E_{PV} from the PV cell v_{PV} and a variable-size energy packet

E_{BAT} from the battery v_{BAT}. f_{PV} and P_{PV} is fixed by the light condition, so when P_{LD} varies the E_{BAT} also varies to provide the requisite battery-assistance P_{SUP} to keep v_O near its target v_{REF}. Transconductor G_{BA} and comparator CP_{BA} in Fig. 4.14 close a pulse-width modulation (PWM) feedback loop about v_O for this purpose, to set how long L_X should energize from v_{BAT}, that is, to set t_{BE} in Fig. 4.3. To regulate v_O about v_{REF}, G_{BA} first amplifies the difference between them and C_{BA} filters it to generate the error signal v_{EA}. Further CP_{BA} translates v_{EA} to t_{BE} by comparing the v_{EA} to a clocked ramp v_R. At the beginning of the ramp v_R, CP_{BA} trips and remains high until v_R exceeds v_{EA} , high pulse at CP_{HS} sets t_{BE}. For example, when load increases, v_{EA} rises and v_R takes longer to reach it, thereby setting a longer t_{BE} and as a result sending a larger battery packet to compensate the higher load.

In this mode the battery can deliver a packet only once after every PV packet. Like in the HS mode the capacitor supplies the load demand in between energy packets since the target photovoltaic frequency is low at 10 KHz the output capacitor is 2.2 µF to provide instantaneous maximum load demands of 1mW.

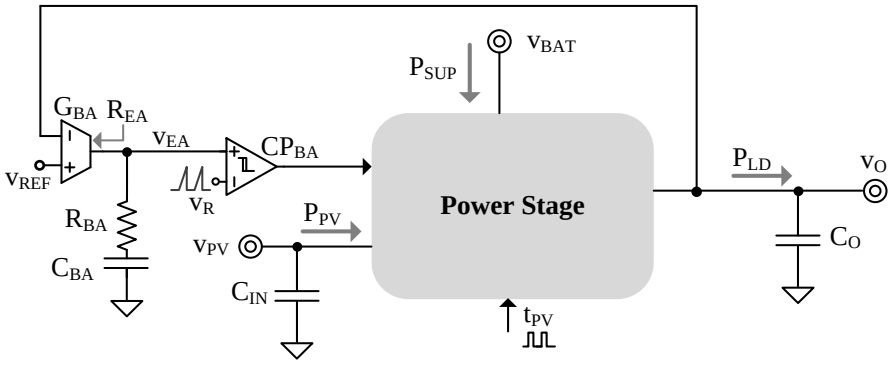


Fig. 4.14. Battery-assisted mode controller for variable size battery packet.

4.3.1.1 Output Ripple

The purpose of capacitor C_O in Fig. 4.13 is to suppress variations in the output voltage v_O. Since the circuit operates in DCM, the C_O receives the total energy load requires in a clock cycle during a short period ($t_{PD}+t_{BE}+t_{BD}$) of the clock cycle. Larger energizing times lead to higher peak current and larger charge in energy packet. Since the circuit delivers all this charge in a short duration larger packets lead to bigger ripple at the output. The series inductance and resistance in the capacitor can also increase the total ripple and the effect is more significant with shorter charge transfer durations.

In the non-reversing circuit at 40-µW P_{PV} and 1-mW P_{LD} the 47-µH inductor takes about a micro second to raise the battery packet peak current to 17 mA and deliver it to C_O. During this time C_O charges and v_O rises 22 mV in Fig. 4.14. Across the rest of the switching cycle, when L_X idles, C_O supplies the load and v_O falls to produce the ripple shown.

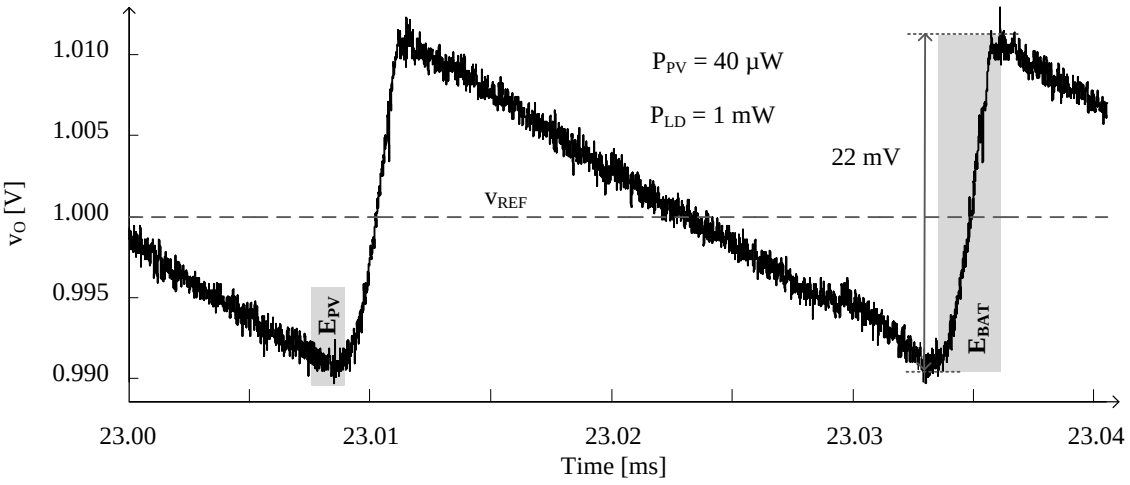


Fig. 4.15. Measured variable packet output when battery-assisted non-reversing circuit.

4.3.1.2 Stability

In the battery assisted mode the system uses a PWM loop to regulate the output voltage about the reference as per the signal flow graph in Fig. 4.15. The transconductance error amplifier G_{BA} amplifies the difference between v_O and v_{REF} with a low frequency gain:

$$A_{EA0} = GM_{EA}R_{EA}. \tag{4.3}$$

Where GM_{EA} is the average transconductance and R_{EA} is the output impedance of G_{BA}. The R_{BA}-C_{BA} filter future smoothens the variations in the amplified voltage. G_{BA}'s output resistance R_{EA} along with R_{BA} and C_{BA} sets the dominant pole at:

$$p_{O1} = \frac{1}{2\pi(R_{EA} + R_{BA})C_{BA}}. \tag{4.4}$$

The frequency dependent gain of the amplifier-filter combination $A_{EA}(s)$ flattens when the R_{BA} dominates C_{BA}'s impedance in their series combination to introduce the phase saving zero:

$$z_{O1} = \frac{1}{2\pi R_{BA}C_{BA}}. \tag{4.5}$$

In this way the $A_{EA}(s)$ translates the small signal perturbation v_O' at output v_O to small signal change v_{ea}. The comparator CP_{BA} then compares v_{ea} with the ramp v_R to set t_{be}. With v_R linearly growing to V_R in T_R duration, the small signal change v_{ea} causes a proportional T_R/V_R change in t_{BE} as in Fig. 4.16.

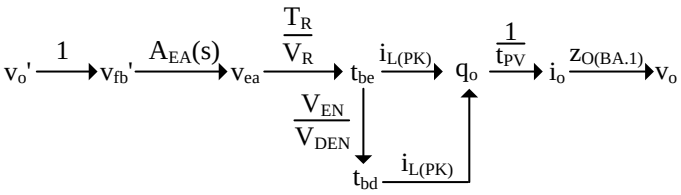


Fig. 4.16. Signal flow graph open loop analysis for variable packet control.

The small signal change t_{be} increases the peak current and thereby the de-energizing time and as a result the charge it delivers in a cycle to the output q_o and the output current i_O in the photovoltaic cycle t_{PV}. The small signal output current i_O flows into the output impedance $Z_{O(BA.1)}$ to correct the initial perturbation at the output and complete the feedback response. The inductor impedance $R_{L.1}$, R_O and C_O defines the output impedance:

$$Z_{O(BA.1)} = R_{L.1} \parallel R_O \parallel \frac{1}{sC_O}, \tag{4.6}$$

and the output pole at:

$$p_{O2} = \frac{1}{2\pi(R_{L.1} \parallel R_O)C_O} \tag{4.7}$$

In Fig 4.17 (a) a small signal circuit models the output impedance circuit that the transfer circuit presents, the inductor connects to the output every cycle for the duration of the PV packet de-energizing time t_{PD} and for the duration of battery packet t_B. A test voltage v_t can ramp the inductor current i_t in during t_{PD} to $i_{T(PK1)}$ and during t_B to $i_{T(PK2)}$. The current returns to zero when the inductor disconnects at the end of the PV packet and battery packet. The ratio of the average test voltage v_t and average test current $i_{t(avg)}$ defines the inductor resistance:

$$R_{L.1} = \frac{v_{T(AVG)}}{i_{T(AVG)}} = \frac{v_T t_{PV}}{\sum_{i=1}^{2} q_{Ti}} = \frac{v_T t_{PV}}{0.5 i_{T(PK1)} t_{PD} + 0.5 i_{T(PK2)} t_B} == \frac{2 L_X t_{PV}}{t_{PD}^2 + t_B^2} \quad (4.8)$$

Where Σq_t is the total charge in every cycle. The design choice of allowing the ramp signal to have constant ramp rate allows the low frequency gain to remain independent of f_{PV} and f_{0dB} to scale with f_{PV} at the cost of tighter input resolution range and noise resolution for the ramp comparator.

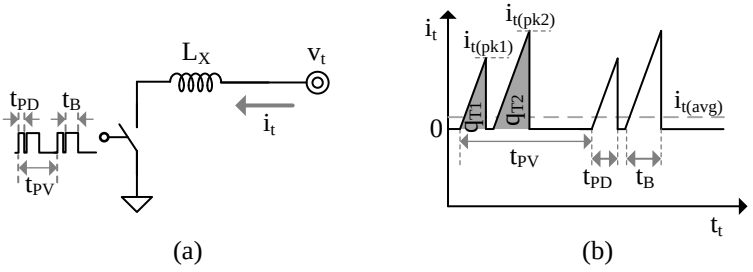


Fig. 4.17. DCM variable-packet small signal output impedance (a) circuit (b) current.

In the non-reversing circuit implementation the low frequency gain of the error amplifier is around 50 dB and R_{EA} is around with 16 MΩ. The external compensating capacitance 2 nF and compensation resistance in 1.2 MΩ sets the dominant output pole at 5 Hz, phase compensating zero at 66 Hz. The output pole moves between 70–300 Hz and near the system's bandwidth f_{0dB} the loop gain falls at -20 dB per decade with close to 70° of phase margin, which means, the loop is stable. C_O's ESR $R_{ESR.O}$ is low and the zero it introduces falls beyond f_{0dB}.

4.3.1.3 Load Regulation

Since L_X idles between deliveries, the full load P_{LD} discharges C_O. So heavier loads pull v_O further. v_O suffers this penalty even after the feedback loop compensates by raising the size of v_{BAT}'s energy packet E_{BAT} because C_O always supplies all of P_{LD} when L_X idles.

This is why v_O's ripple increases with heavier loads in Fig. 4.18. In the non-reversing implementation, with P_{PV} of 100 µW, the peak to peak output ripple increases from 5 mV to 12 mV with i_{LD} varying from 500 µW to 1.1 mW.

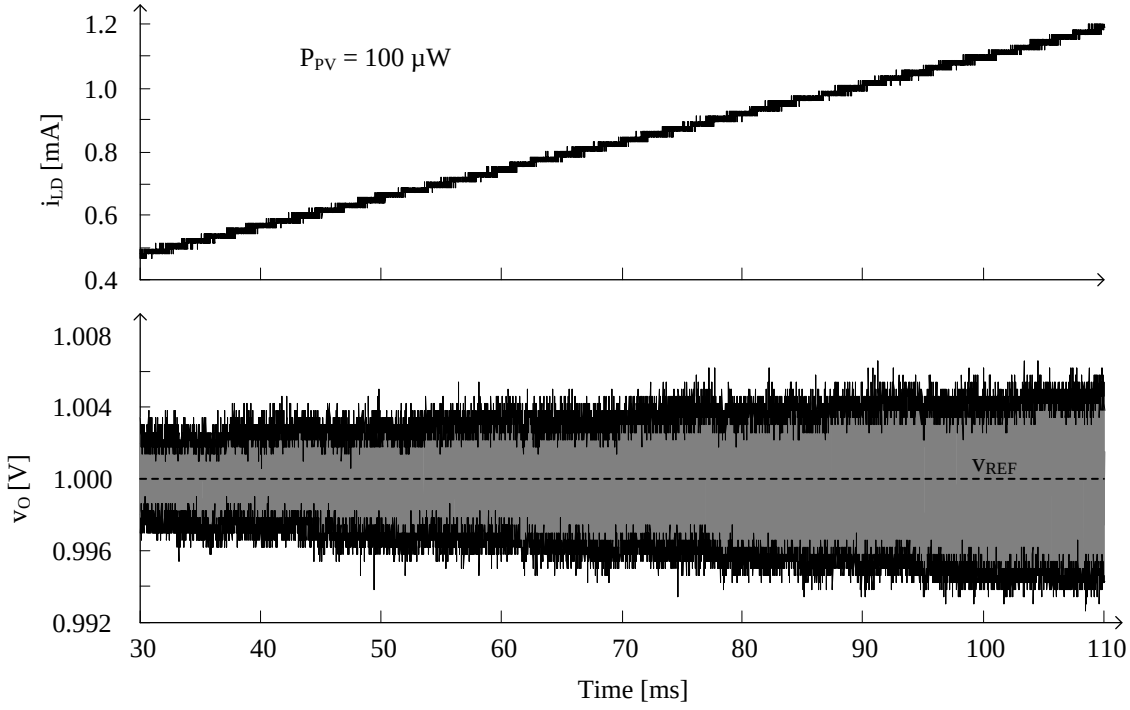


Fig. 4.18. Measured variable packet output when load climbs.

Figure 4.19 shows the response of output to rising and falling load dumps. At 12.5 ms the load current drops from 800 µA to 400 µA within a 1 µs, the 15-mA peak current steady sate battery packets overwhelm the output for period and the output overshoots to 15 mV above the reference. This causes v_{EA} to drop and the battery packets size reduces, the load current overwhelms the charge that the smaller battery packets drops and the output drops towards the reference value. As the output nears the reference value the v_{EA} adjusts such that the battery packets provides just enough charge to balance the load every cycle. Finally around 17 ms the output reaches new steady state with the system

delivering 10-mA battery packets every cycle. The dynamics reverse for the rising load dump at 30 ms here the large load current discharges the output to a ripple offset of 25 mV before the controller responds the next cycle to correct the error. In this case system sends very large packets of energy initially and then settles smoothly to the steady state value of 15-mA peak current. In response to the load step the output settle smoothly back to the steady state value without any ringing validating at 90° phase margin stable response.

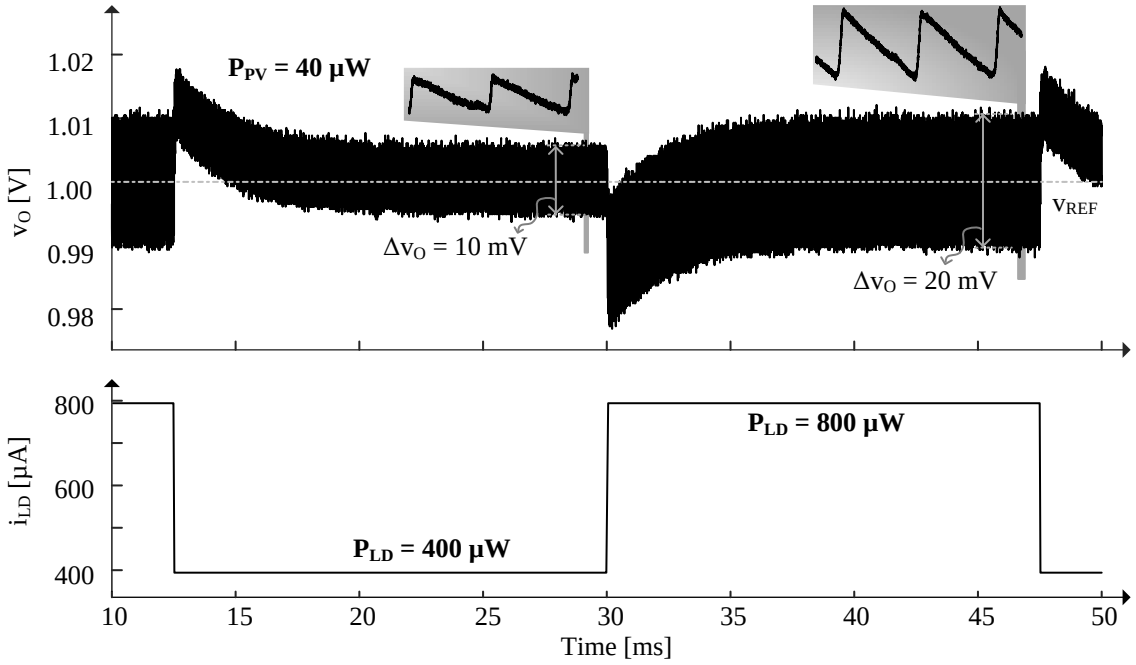


Fig. 4.19. Measured rising and falling load dump response at output.

4.3.2 Multiple Packets

In battery-assisted mode, the P_{PV} is insufficient to supply P_{LD}, therefore output v_O receives a fixed energy packet E_{PV} from the PV cell v_{PV} and multiple fixed size E_{BAT} energy packets from the battery. f_{PV} and P_{PV} is fixed by the light condition, and E_{BAT} is

fixed by design so when P_{LD} varies the number of packets n_B varies to provide the requisite battery-assistance P_{SUP} to keep v_O near its target v_{REF}. Transconductor G_{BA} and comparator CP_{BA} in Fig. 4.20 close a pulse-width modulation (PWM) feedback loop about v_O for this purpose, to set how long L_X should transfer energy packets from v_{BAT}, that is, to set n_B in Fig. 4.4.

To regulate v_O about v_{REF}, G_{BA} first amplifies the difference between them and C_{BA} filters it to generate the error signal v_{EA}. Further CP_{BA} translates v_{EA} to t_{ON} by comparing the v_{EA} to a clocked ramp v_R. At the beginning of the ramp v_R, CP_{BA} trips and remains high until v_R exceeds v_{EA} , high pulse at CP_{HS} sets t_{ON}. As long as the t_{ON} is high the latch and it delayed-reset sends fixed-size pulse every time a inductor current crosses to zero indicating the end of a packet the fixed size pulse sets the battery packet energy time and as a result system delivers a fixed size energy packet. For example, when load increases, v_{EA} rises and v_R takes longer to reach it, thereby setting a longer t_{ON} and as a result sending a larger number of battery packets to compensate the higher load.

In this mode the battery can deliver multiple packets after every PV packet. But once the t_{ON} goes low the system has to wait for the next photovoltaic cycle to start sending packets again. Like in the HS mode the capacitor supplies the load demand in the period of no conduction since the target photovoltaic frequency is low at 10 kHz the output capacitor is 10 µF to provide instantaneous maximum load demands of upto 5mW.

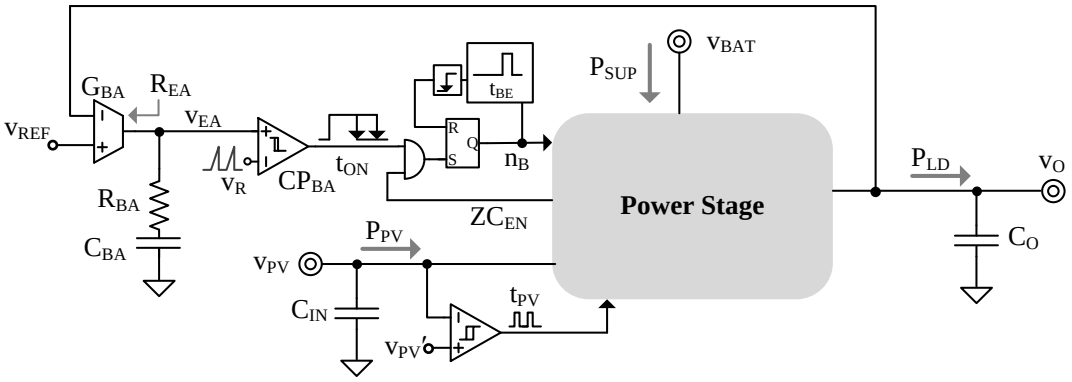


Fig. 4.20. Battery-assisted mode controller for multiple fixed-size battery packets.

4.3.2.1 Output Ripple

In the reversing power transfer circuit, Fig. 4.20, the output receives a photovoltaic packet and multiple battery packets every clock cycle. The multiple energy packets from the battery dominates the load and raises the output every cycle but the load discharges the output during the rest of the cycle. Since the battery energy every cycle is a positive integer multiple of E_{BAT}, generally the battery power is either greater or smaller than the load demand. The system switches between sending larger or smaller number of packets every cycle to on an average meet the output demand over multiple cycles. This leads to limit cycling at the output where the number of packets is not constant from cycle to cycle and the output has an overriding low frequency content. This is unlike the variable packet scheme that satisfies load demand every cycle and as a result the output frequency was the same as f_{PV}.

In the Fig. 4.21 the peak-to-peak output ripple across a 10-µF capacitor with P_{PV} at 130 µW and P_{LD} of 10 mW is 4 mV. The systems supplies 6 battery packets to v_O between 5 ms and 10 ms and, 7 packets for the PV cycles of 15–37 ms. As a result the

output rises about 1 mV when n_B is 7 and drops 2 mV when n_B is 6. Across a 7-packet t_{PV} period the output rises by about 4 mV when the system supplies energy and the 10 mA load discharge most of it during the period of no conduction. The maximum number of packets depends on the t_{PV} and can vary between 0–70 at 10-µW P_{PV}. As the photovoltaic frequency decrease with P_{PV} the period of no conduction can increase and so the output ripple also increases.

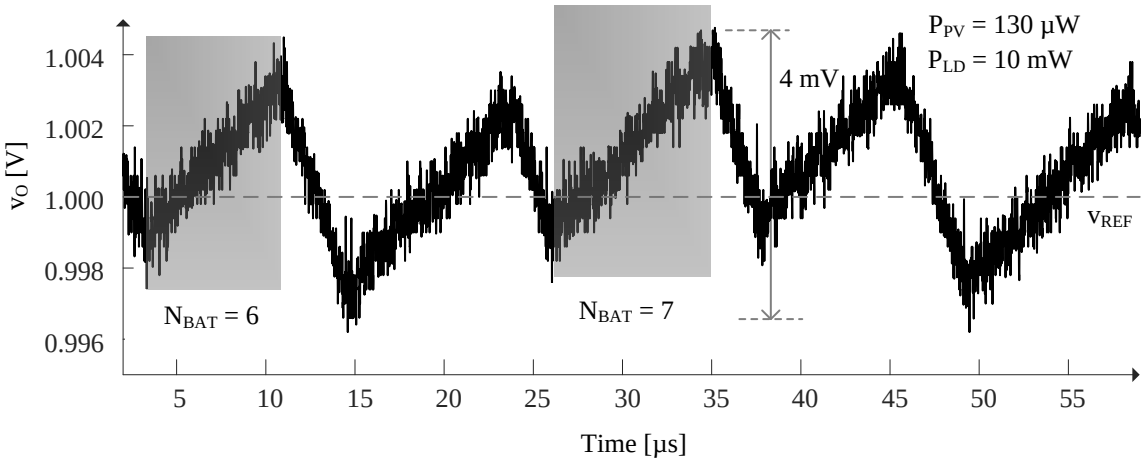


Fig. 4.21. Measured multiple packets output when battery-assisted reversing circuit.

4.3.2.2 Stability

In the battery assisted mode the multiple packet system uses a digitized-PWM loop to regulate the output voltage about the reference as per the signal flow graph in Fig. 4.21. The transconductance error amplifier G_{BA} amplifies the difference between v_O and v_{REF} with a low frequency gain:

$$A_{EA0} = GM_{EA}R_{EA}\,, \tag{4.3}$$

where GM_{EA} is the average transconductance and R_{EA} is the output impedance of G_{BA}. The R_{BA}-C_{BA} filter future smoothens the variations in the amplified voltage. G_{BA}'s output resistance R_{EA} along with R_{BA} and C_{BA} sets the dominant pole at:

$$p_{O1} = \frac{1}{2\pi(R_{EA} + R_{BA})C_{BA}}. \tag{4.4}$$

The frequency dependent gain of the amplifier-filter combination $A_{EA}(s)$ flattens when the R_{BA} dominates C_{BA}'s impedance in their series combination to introduce the phase saving zero:

$$z_{O1} = \frac{1}{2\pi R_{BA} C_{BA}}. \tag{4.5}$$

In this way the $A_{EA}(s)$ translates the small signal perturbation v_O' at output v_O to small signal change v_{ea}. The comparator CP_{BA} then compares v_{ea} with the ramp v_R to set t_{be}. With v_R linearly growing to V_R in T_R duration, the small signal change v_{ea} causes a proportional T_R/V_R change in t_{ON} as in Fig. 4.22.

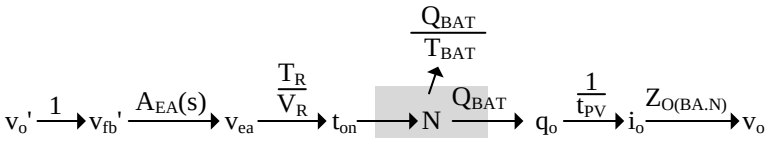


Fig. 4.22. Signal flow graph open loop analysis for multiple packets.

To apply to signal flow analysis to the digitized-PWM loop Fig. 4.22 linearizes the translation from t_{ON} to the small signal output charge q_O by approximating the nonlinear step relationship in Fig. 4.22 with the gray line representing a linear relation. As a result

the q_o/t_{on} can approximate to ratio of a single battery packet charge Q_{BAT} to the duration it takes to conduct t_{BAT} as the relation in Fig. 4.23 highlights. Further the small signal change in charge q_o over every PV cycle t_{PV} defines the change in output current i_o.

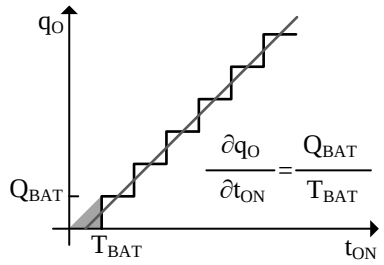


Fig. 4.23. Small signal output charge to PWM on-time.

The small signal output current i_O flows into the output impedance $Z_{O(BA.N)}$ to correct the initial perturbation at the output and complete the feedback response. The inductor impedance $R_{L.N}$, R_O and C_O defines the output impedance:

$$Z_{O(BA.N)} = R_{L.N} \parallel R_O \parallel \frac{1}{sC_O}, \tag{4.6}$$

and the output pole at:

$$p_{O2} = \frac{1}{2\pi(R_{L.N} \parallel R_O)C_O}. \tag{4.7}$$

In Fig 4.24 (a) a small signal circuit models the output impedance circuit that the transfer circuit presents, the inductor connects to the output every cycle for the duration of the PV packet de-energizing time t_{PD} and for the duration of every battery packet t_B. A test voltage v_t can ramp the inductor current i_t in during t_{PD} to $i_{T(PK1)}$ and during t_B period of each of n_B packet to $i_{T(PK2)}$. The current returns to zero when the inductor disconnects

at the end of the PV packet and battery packet. The ratio of the average test voltage v_t and average test current $i_{t(avg)}$ defines the inductor resistance:

$$R_{L.N} = \frac{v_{T(AVG)}}{i_{T(AVG)}} = \frac{v_T t_{PV}}{\sum_{i=1}^{n_B} q_{Ti}} = \frac{v_T t_{PV}}{0.5 i_{T(PK1)} t_{PD} + 0.5 i_{T(PK2)} t_B} == \frac{2 L_X t_{PV}}{t_{PD}^2 + n_B t_B^2} \qquad (4.8)$$

Where Σq_t is the total charge in every cycle as Fig. 4.25 (b) shows. The design choice of allowing the ramp signal to have constant ramp rate allows the low frequency gain to remain independent of f_{PV} and f_{0dB} to scale with f_{PV} at the cost of tighter input resolution range and noise resolution for the ramp comparator.

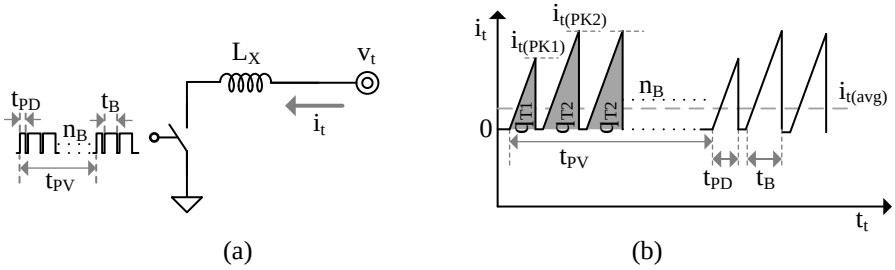


Fig. 4.24. DCM multiple-packet small signal output impedance (a) circuit (b) current.

In the reversing circuit implementation the low frequency gain of the error amplifier is around 55 dB and R_{EA} is around with 100 MΩ. The external compensating capacitance 75 pF and compensation resistance in 2 MΩ sets the dominant output pole at 20 Hz, phase compensating zero at 1.5 kHz. The output pole moves between 200–1200 Hz and near the system's bandwidth f_{0dB} the loop gain falls at -20 dB per decade with close to 50° of phase margin, which means, the loop is stable. C_O's ESR $R_{ESR.O}$ is low and the zero it introduces falls beyond f_{0dB}. In this case the output pole comes before the phase saving zero therefore the phase dips about 160° near 1 kHz but recovers back towards 90° with the effect of the phase saving zero.

4.3.2.3 Load Regulation

Figure 4.25. shows the response of output to rising and falling load dumps. At 13 ms the load current drops from 2 mA to 1 mA within a 1 µs, the 15-battery packets each of 27-mA peak current in steady sate overwhelm the output for the next few period before output settle to the new steady state. This causes v_{EA} to drop and the number of battery packets reduces, the load current overwhelms the charge that the smaller number of battery packets provides and the output drops towards the reference value. As the output nears the reference value v_{EA} adjusts such that the battery packets provides just enough charge to balance the load every cycle. Finally around 13.5 ms the output reaches new steady state with the system delivering 7 battery packets every cycle. The dynamics reverse for the rising load dump at 3 ms here the large load current discharges the output to a ripple offset of 25 mV before the controller responds the next cycle to correct the error. In this case system sends large number of packets initially and then settles smoothly to the steady state value of 15. In response to the load step the output settle smoothly back to the steady state value with less than 3 rings validating a more than 60° phase margin stable response.

The number of packets as the earlier section mentions is not steady and cycles between 6–7 in case of 1 mA load current and 14–17 in case of 2 mA load current condition at steady state. This cases a low frequency ripple at the output which the output capacitor C_O filters. The overshoot and under shoot reduces at higher P_{PV} and the corresponding f_{PV} as the system engages faster in this instance.

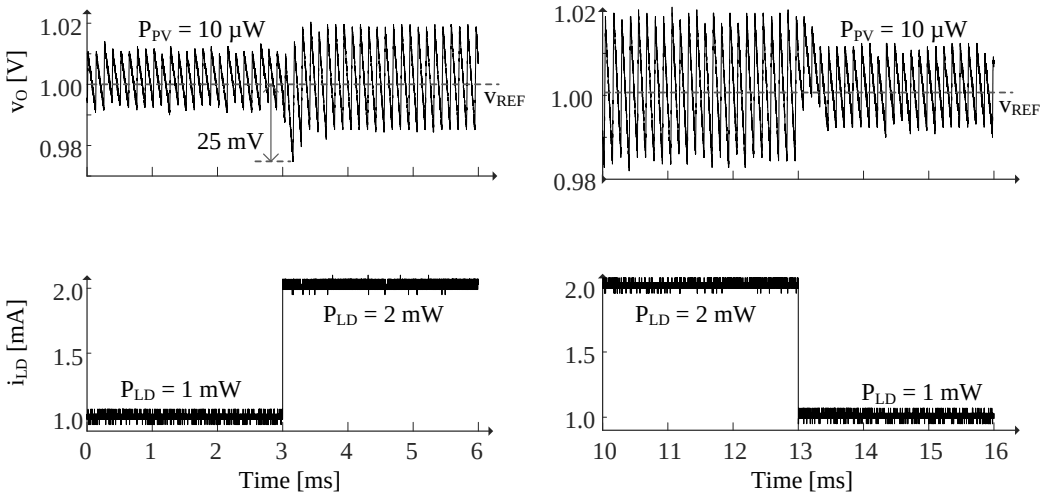


Fig. 4.25. Measured output load dump response for multiple-packet scheme.

4.4 Mode Transition

Hysteretic comparator CP_M in Fig. 4.26 monitors v_O to determine which mode of operation the system adopts in response to load transients. While in heavily sourced if the load suddenly ramps greater than P_{PV}, the v_O falls even when Pv packets reach the the ouput every cycle. The mode comparator CP_M has a threshold V_{HYSM-} that is lower than CP_{HS}'s and when v_O fall V_{HYSM-} below v_{REF} the system switches mode to battery assistance and the output recovers with assistance from battery. Similarly while in receiving battery assistance the load falls below P_{PV}, the output continue to rise even when no battery packet reaches it. When the output rises V_{HYSM+} the system switches the mode to heavily-sourced and steers the PV packets to battery and letting the load discharge the output to v_{REF}. The mode controller thus implements an external hysteric window and when the output exceeds the upper threshold mode switches to heavily-sourced and when v_O falls below the lower threshold mode switches to battery-assisted.

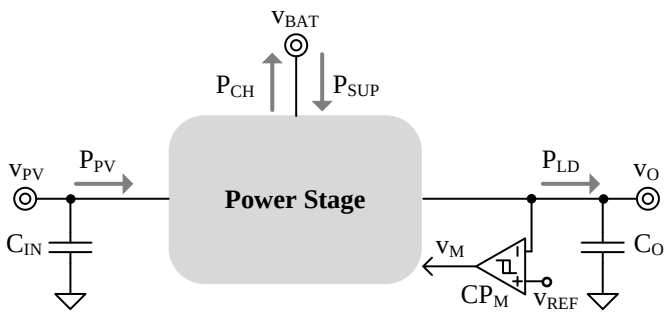


Fig. 4.26. External hysteretic controller that implements mode control.

4.4.1 Variable Packet

4.4.1.1 Output Ripple

When P_{LD} slightly exceed PV power P_{PV}, the network can switch back and forth between modes. The reason for this that the switching network can't switch fast enough to deliver an arbitrarily small packet. In Fig. 4.27 v_O drops at 3.2 ms even when all the PV packets are directed to it, as P_{LD} is 20 µW higher than P_{PV}. v_O continues to drop until the it hits the lower threshold of CP_M, when operation translates to battery-assisted mode and battery starts delivering packets. As v_O recovers and rises with battery assistance, and size of battery packets decrease but even the smallest E_{BAT} along with P_{PV} exceeds P_{LD}, therefore v_O continues to rise beyond v_{REF}. Eventually at 7.2 ms v_O exceeds the upper threshold of CP_M and system switches back to heavily sourced mode. Except again, P_{LD} overloads P_{PV}, v_O falls back, and the process repeats until P_{LD} is high enough to sink all of the power that v_{PV} and v_{BAT} supply.

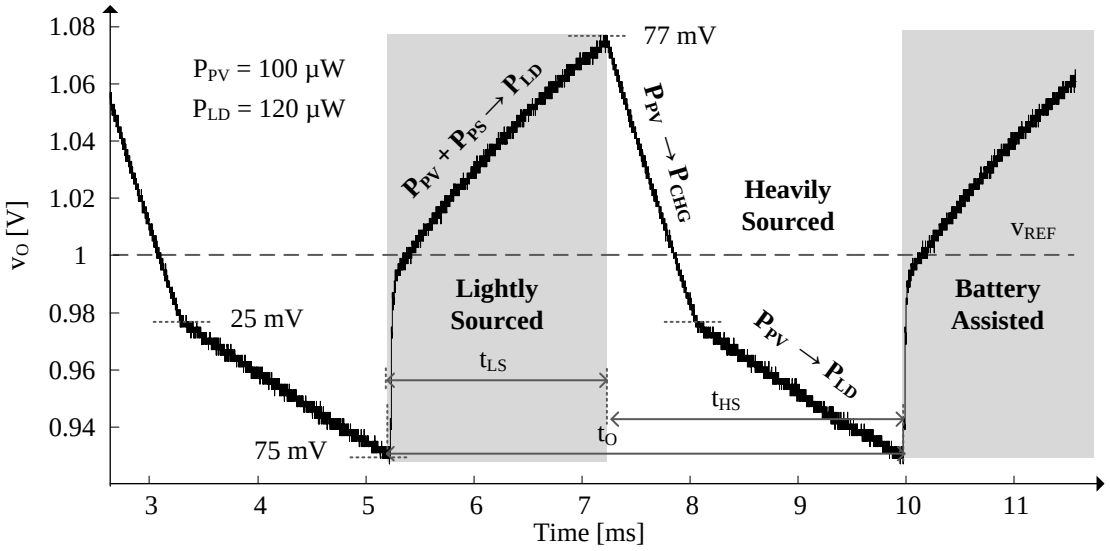


Fig. 4.27. Measured output when load power just exceeds PV power for variable-packet.

4.4.1.2 Load regulation

Fig. 4.28 shows the region where mode transition mode occurs and how the output period varies. In HS mode, as P_{LD} increases, it is difficult or more time consuming to charge the output as the discharging current is high. As a result, in Fig. 10, t_O increases from 2.6 ms to 9.2 ms as the P_{LD} increase from 60 µW to 80 µW. As P_{LD} increases past 80 µW, P_{PV} at 100 µW after losses is not sufficient to satisfy the load and requires battery-assistance. t_O peaks to 21 ms at 90 µW load, since the output regulation threshold is larger at ± 77mV during mode transition and P_{LD} discharges the output slowly when P_{PV}, which is close to P_{LD}, is redirected to the output. As P_{LD} gets larger than P_{PV}, it can discharge the output faster, t_O decreases. However t_O increases beyond 140-µW, as battery-assistance time t_B becomes a larger fraction of t_O. Past 160 µW, circuit draws assistance from battery every cycle and satisfies the load in a single switching cycle, as a result t_O reduces to t_{PV}.

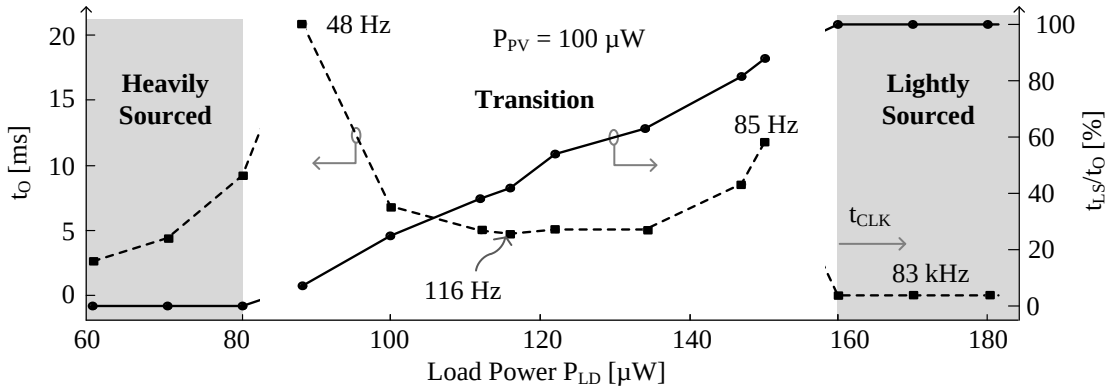


Fig. 4.28. Measured mode control output period across load level.

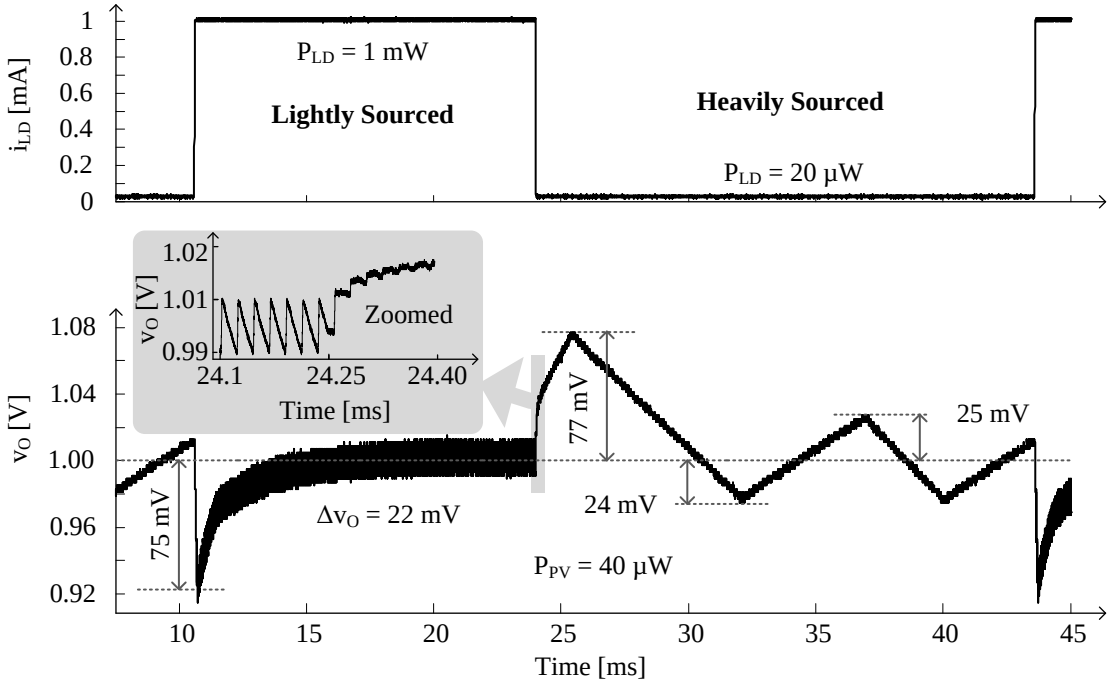


Fig. 4.29. Measured rising and falling load dump response at output.

Hysteretic comparator CP_M in Fig. 4.29 monitors v_O to determine which mode of operation the system adopts in response to load transients. For example, while in heavily sourced mode, when P_{LD} increases beyond P_{PV}, v_O falls even when the system diverts all the PV cell packets to it. v_O continues to fall beyond the lower threshold of the CP_{HS} and hits lower threshold of CP_M when v_M rises to shift the mode to battery-assisted condition,

as Fig.4.29 shows at 11 ms. Further after v_M flips, PWM loop engages to send large packets of energy from battery and v_O recovers to settle around 1V.

On the other hand, when the system is in battery-assisted mode and the P_{LD} drops below P_{PV}, v_O rises as packets from both PV cell and battery overwhelm P_{LD}. The PWM loop reduces the size of E_{BAT} as v_O rises and eventually sends minimum size packets to the battery. However, packets from the PV cell and minimum size packets from the battery overwhelm P_{LD} and vo rises until it hits the upper threshold of CP_M then v_M trips and system switches to heavily source mode. Once in heavily sourced mode, the system initially steers all the PV packets to battery until P_{LD} discharges v_O to lower threshold of CP_{HS}, when inner hysteretic loops regulates it.

Mode comparator CP_M has a short propagation delay and reacts to large changes in P_{LD} within a clock cycle. If P_{LD} increases suddenly and v_O falls 75 mV below v_{REF}, CP_M sets the system to battery-assisted response and when v_O rises above 77 mV in response to load changes CP_M moves the system to heavily source mode. In Fig. 4.29, for example, v_O falls quickly when P_{LD} rises from 20 μW to 1 mW at 11 ms. But as soon as v_O falls 75 mV below 1 V, CP_M shifts the system into the battery-assisted region. In this mode, energy packets from the battery arrest and reverse v_O's fall. E_{BAT}'s similarly raise v_O after P_{LD} drops from 1 mW to 20 μW at 24 ms. But when v_O rises 77 mV above 1 V, CP_M shifts mode to, again, arrest and reverse the rise.

4.4.2 Multiple Packets

4.4.2.1 Load regulation

Mode comparator CP_M has a short propagation delay and reacts to large changes in P_{LD} within a clock cycle, the regulation is similar to the variable packet scheme. If P_{LD} increases suddenly and v_O falls 60 mV below v_{REF}, CP_M sets the system to battery-assisted response and when v_O rises above 60 mV in response to load changes CP_M moves the system to heavily source mode.

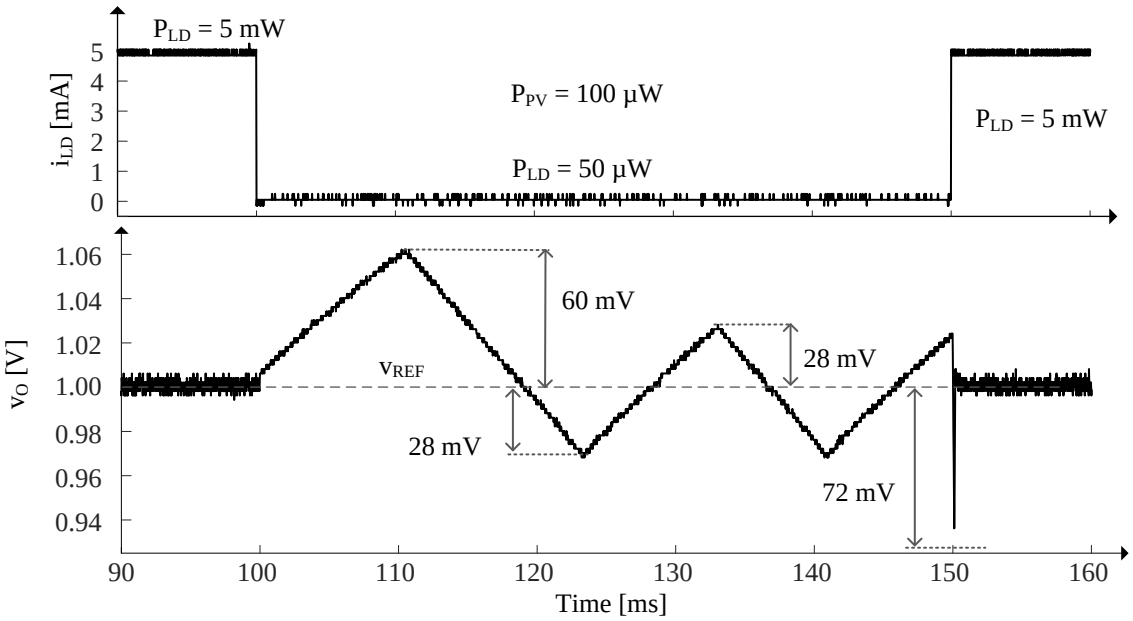


Fig. 4.30. Measured rising and falling load dump response at output.

In Fig. 4.30, for example, v_O falls quickly when P_{LD} rises from 50 µW to 5 mW at 150 ms. But as soon as v_O falls 60 mV below 1 V, CP_M shifts the system into the battery-assisted region. In this mode, energy packets from the battery arrest and reverse v_O's fall. E_{BAT}'s similarly raise v_O after P_{LD} drops from 10 mW to 50 µW at 100 ms. But when v_O rises 60 mV above 1 V, CP_M shifts mode to, again, arrest and reverse the rise. The

reversing implementation has a higher bandwidth by design and as a result the output settles faster to the reference value in comparison than in the non-reversing case.

4.5 Summary

The chapter presents feedback control for the non-reversing and reversing charger–supply power stages. The non-reversing power stage implements a variable battery packet battery-assistance control scheme and the reversing circuit implements the multiple battery packet control scheme. Both circuits employ an inner hysteretic control in heavily-sourced mode and external hysteretic control scheme for mode switching. The maximum steady state voltage ripple is less 2.5 % of the reference 1V in both the cases and less than 7.5% across load dumps. Both the control scheme provides a robust output voltage of around 1V while transferring up to 1 mW in case of variable packet and 10 mW in case of multiple packet control scheme. The bandwidth in case of the multiple packet control scheme is slightly better than the variable packet scheme and as a result the response time is faster for the multiple packet scheme.

CHAPTER 5. CMOS IMPLEMENTATION

CMOS fabrication technology allows for the integrated implementation of the power stage options in Chapter 3 and the controller options in Chapter 4. The major consideration in integrated implementation is the reducing losses and area of the implementation. The rest of chapter shows the design of the two different power stages reversing and non-reversing and the control blocks that implement the feedback control, variable packet control for non-reversing case and multiple packet control for the reversing case. The non-reversing switching circuit transfers 10–100 µW photovoltaic power to the output and up to 1 mW battery power to the output while recharging battery with excess PV power. This circuit scales the frequency of PV packets with P_{PV} and size of the battery packet with P_{LD}. Meanwhile the reversing switching circuit higher power levels of 10–130 µW photovoltaic power to the output and to 10 mW battery power to the output and also recharges the battery with excess PV power. This circuit scales the frequency of PV packets with P_{PV} and number of fixed-size battery packets with P_{LD}.

5.1 Non-Reversing CMOS Charger–Supply

5.1.1 System

The photovoltaic power switch M_{PV}, the photovoltaic ground switch M_{G2}, output switch M_{O1} and M_{O2}, the battery charging switch $M_{B(CHG)}$ and battery-assistance switch $M_{B(AID)}$ implements the non-reversing power stage in Fig. 5.1. M_{PV} and M_{G2} close to energize the inductor L_X from photovoltaic voltage v_{PV} to ground. M_{O1}, M_{O2} and M_{PV} close to drain the inductor from v_{PV} to output v_O, thereby supplying photovoltaic power to v_O. Similarly

M_{PV} and $M_{B(CHG)}$ close to drain L_X from v_{PV} to battery v_{BAT}, and charge the battery with excess photovoltaic power. M_{O1}, M_{O2} and $M_{B(AID)}$ close to energize L_X from v_{BAT} to v_O. M_{O1}, M_{O2} and M_{G1} can close to drain the remaining battery energy to v_O. For higher efficiency at low power levels the circuit operates in DCM, M_{NR} is the ring kill switch engages when all the switches close to dissipate remnant inductor energy after power transfers.

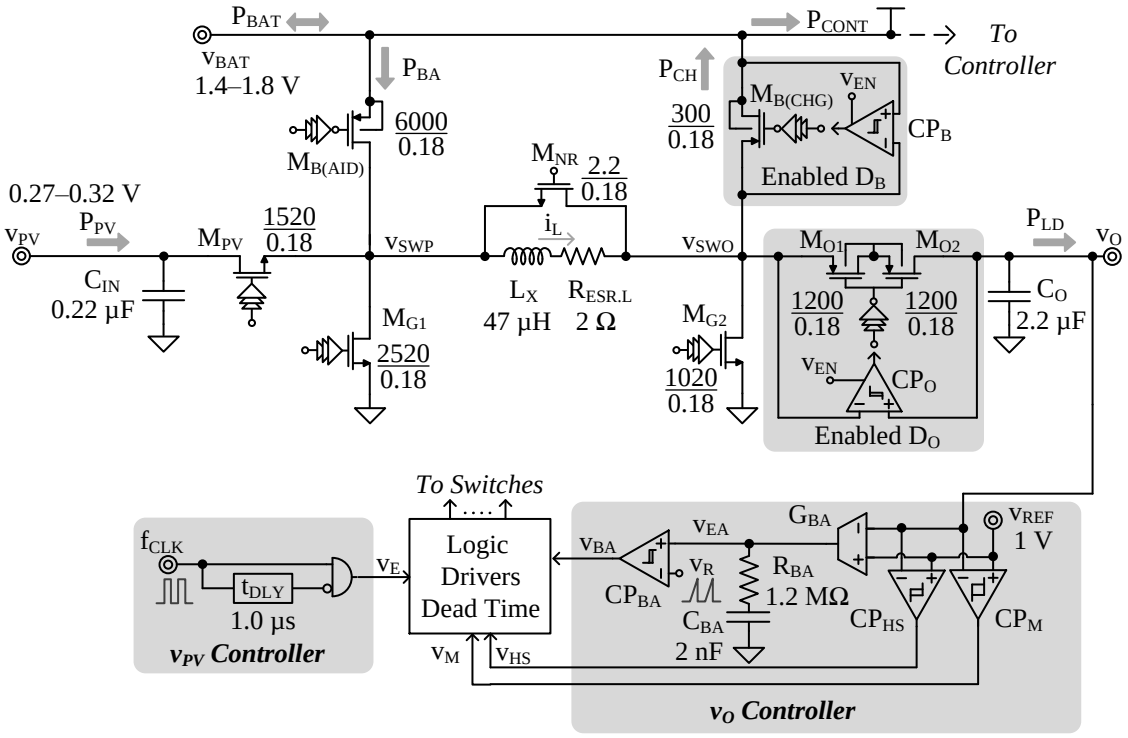


Fig. 5.1. Non-reversing switched-inductor charger–supply CMOS implementation.

The control blocks in Fig. 5.1 processes voltages and currents and along with the logic block generates switching signals for the power stage. The major blocks in the design, in Fig. 5.1, are error amplifier G_{BA}, battery-assist comparator CP_{BA}, heavily source comparator CP_{HS}, mode-detect comparator CP_M and the diode comparators CP_O and CP_B. CP_B and CP_O are diode comparators that digital logic can enable to measure

voltage across switches $M_{B(CHG)}$ and M_{O1}-M_{O2} and turn of the respective switches when inductor depletes. CP_{HS} is the inner hysteretic comparator that compares v_O and the reference voltage v_{REF} to determine the direction of energy flow in heavily-sourced mode. The battery-assist transconductor G_{BA} amplifies the difference between v_O and v_{REF} that the filter R_{BA}-C_{BA} filters to generate error voltage v_{EA}. The battery-assist comparator CP_{BA} compares v_{EA} and the ramp signal v_R to generate the energizing time of the battery packet. An external maximum power point frequency clock sets the frequency of the PV packets and the fixed 1-µs delay block sets the energizing time of the PV packet.

The 0.18-µm CMOS non-reversing variable size battery packet integrated circuit (IC) along with the test circuitry occupies 610 × 610 μm^2 in Fig. 5.2. This system transfers between 10–100 µW photovoltaic power and remaining battery power to supply upto 1-mW load and charge battery with extra PV power. The power switches occupy about 20% of the IC. In the layout location of the switches, pins and the orientation of the metal connections to drain and source are important considerations that reduce the series path resistance. For example the leftmost pad on the bottom side connects to the battery pin and the second pad from left on the bottom side is the photovoltaic switching node v_{SWP}, therefore placement of $M_{B(AID)}$ at the left bottom corner between the pins reduces the series path resistance. The layout allots highest placement priority to higher power carrying switches by placing them close to the pins. The major considerations that determine the placement of the control block are noise sensitivity, interconnects supply routing. The placement of the diode comparators CP_B and CP_O are close to the respective switches. The comparators shield the noise sensitive error amplifier and bias block from the digital noise. The delay block occupies a lot space due to the large area capacitors

scaling down the charging current can reduce the capacitor size at the cost of higher noise sensitivity.

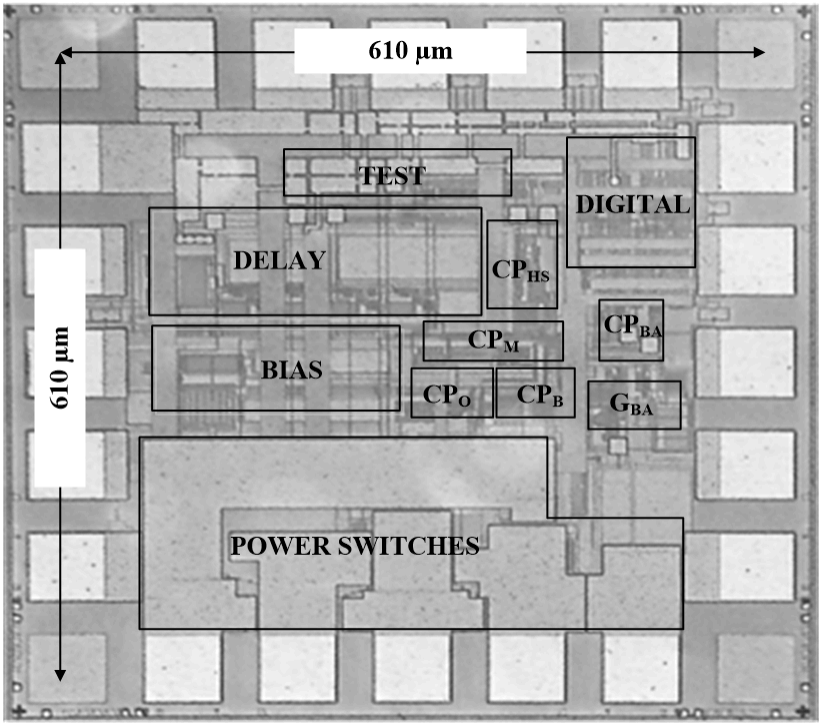


Fig. 5.2. Non-reversing switched-inductor charger–supply die photograph.

5.1.2 Controller Circuits

5.1.2.1 Heavily Sourced Comparator

The heavily sourced comparator CP_{HS} in Fig. 5.1 monitors v_O and regulates it around v_{REF}. A two stage amplifier in open loop implements the comparator in Fig. 5.3. The transconductance of M_{10} and M_{11} that operate near subthreshold amplifies the voltage difference between v_{REF} and v_O into a current, M_{12}–M_{21}, M_{13}–M_{14}, M_{15}–M_{16} mirrors the current and, the output impedance of M_{21} and M_{16} translate the current to a single ended full swing output. The inverter M_{28}–M_{29}, M_{30}–M_{31} and M_{32}–M_{33} buffers the signal to the output v_{HS}.

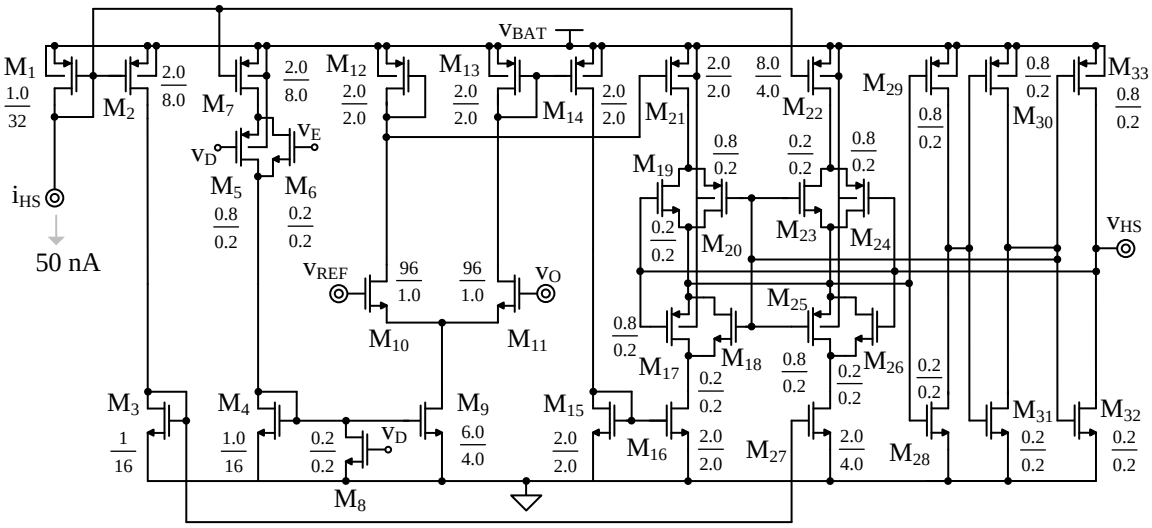


Fig. 5.3. Non-reversing heavily sourced comparator.

The output v_{HS} sources or sinks a hysteretic current via M_{22} or M_{27}. Therefore when the output changes it takes effort to switch back. This way the v_{HS} trips low when vo rises 25 mV above v_{REF} and trips high when v_O falls 24 mV below v_{REF}. The digital switches M_5, M_6 and M_8 can disable the current paths to power gate the block when CP_{HS} is not in use. The comparator turns on only in the HS mode during the energizing time of E_{PV}, makes the decision on the direction to send E_{PV} and then turns off. The digital logic samples and latches v_{HS} before it turns off and retains v_{HS} when CP_{HS} turns back on via v_{OSB}. M_1, M_2, M_3, M_4, M_7 and M_9 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage. The comparator consumes around 15 µA current when it is on. As the comparator needs to make a decision mid-way through the E_{PV} energizing time of 1 µs it has a delay of less than 250 ns for 2 mV overdrive.

5.1.2.2 Battery-Assist Transconductor

The battery-assist transconductor G_{BA} in Fig. 5.1 amplifies the voltage difference between v_O and v_{REF} to output v_{EA}. The transconductance amplifier in Fig. 5.4 implements G_{BA}. The transconductance of M_6 and M_7 that operate near subthreshold amplifies the voltage difference v_O and v_{REF} into a current. M_8–M_{19}, M_9–M_{10} and M_{14}–M_{16} mirror the current difference to the output node v_{EA}. The output impedance of the M_{16} and M_{19} translate the current to the single ended output v_{EA}. M_1, M_2, M_3 and M_5 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage.

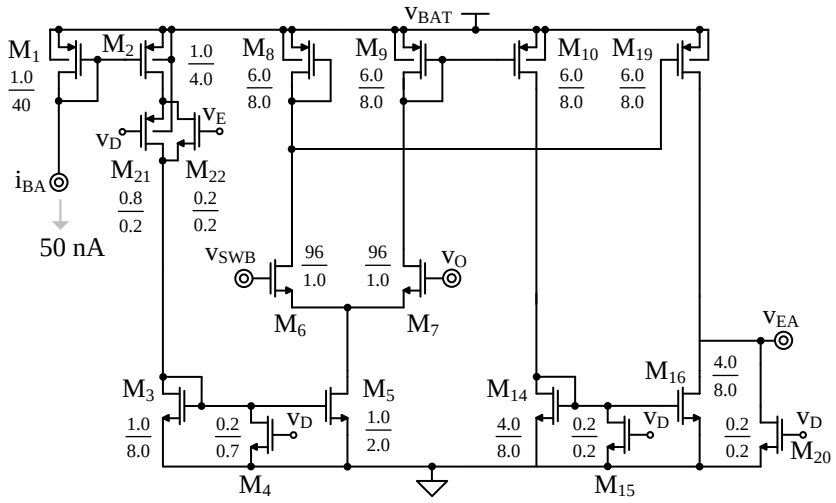


Fig. 5.4. Non-reversing battery-assist transconductor.

The digital switches M_{21}, M_{22}, M_4, and M_{15} can disable the current paths to power gate the block when G_{BA} not in use. The transconductor block turns on only during battery-assistance mode. The non-reversing circuit, in Fig. 5.1, has an external compensation where v_{EA} node is bonded out and the dominant pole is set by a large external cap of 2nF and 10-MΩ output impedance of G_{BA} and R_{BA} resistance of 1.2 MΩ

adds the phase saving zero. In the case the gain of G_{BA} is greater than 40 dB across all temperature and process corners.

5.1.2.3 Ramp Generator

In the PWM loop the transconductor amplifier amplifies the voltage difference between the output and reference to generate the error voltage v_{EA}. To control the energy flow from source to load on the basis of this error the controller needs to convert the error voltage to a timing signal that turns controls in the on/off time of the switches that energizes and drain L_X. Comparing the error voltage with a voltage, which ramps linearly from a low to high value with time, is one method to translate v_{EA} to a timing signal. In the variable size battery packet control the timing signal sets the on time of the battery packet and in the multiple packets it sets the duration for which the battery packets are sent. To generate the ramp signal the ramp generator circuit in Fig. 5.5 charges a capacitor with a constant current. In Fig 5.1 the ramp generator circuit turns on at the end of the PV packet. M_1 and M_2 mirrors the 50 nA bias current i_R to charge the capacitor voltage v_R as soon as the circuit turns on. The digital switches M_3 and M_4 can disable the current path to power gate the block the ramp generator.

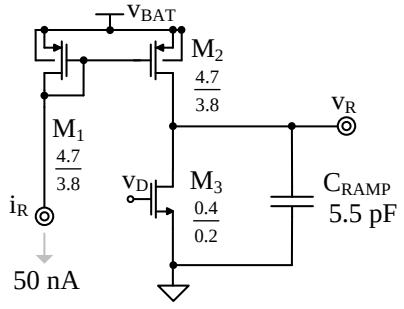


Fig. 5.5. Non-reversing ramp generator.

5.1.2.4 Battery-Assist Comparator

The battery-assist comparator CP_{BA} in Fig 5.1 compares the error voltage v_{EA} and ramp signal v_R to set the energizing time for variable size battery packet or the on-time for the multiple packet case. The two stage amplifier in Fig 5.6 in open loop implements the CP_{BA} comparator. The transconductance gm_I of M_8 and M_9, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{EA} and v_R into a current. M_{10}–M_{12}, M_{11}–M_{20} and M_{15}–M_{17} mirrors the current and, the output impedance of M_{17} and M_{20} translate the current to the single ended output that drives the gates of the inverter M_{24}–M_{25}. The inverters M_{26}–M_{27} and M_{28}–M_{29} buffer the signal to the output v_{ON}.

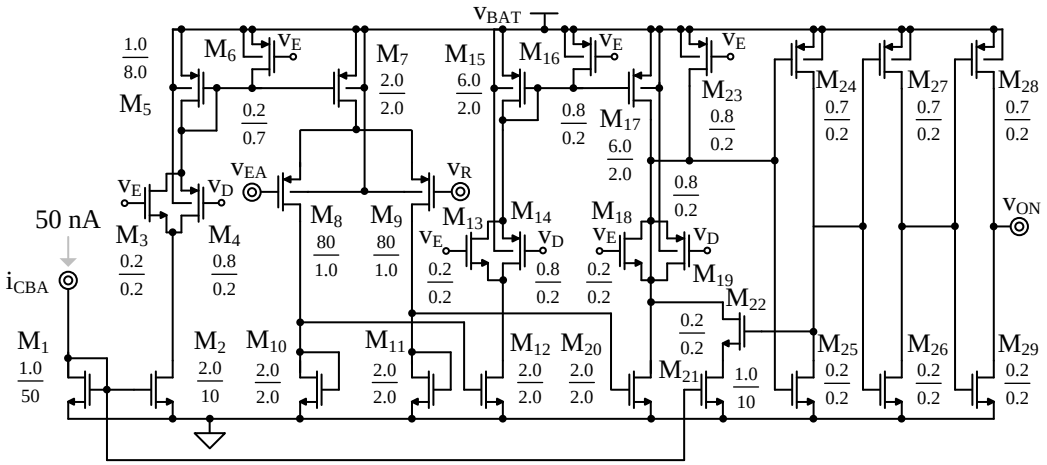


Fig. 5.6. Non-reversing battery-assist comparator.

With the output of the inverter M_{24}–M_{25} high, M_{22} engages M_{21} to further pull M_{24}–M_{25}'s gate low and reinforce the high state at its output. This way M_{21} sets a 5 mV hysteresis so that v_{ON} doesn't shuttle back and forth with noise at v_R or v_{EA} around the trip point. M_1–M_2 and M_6–M_7 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage. The comparator has a

delay of less than 200 ns for an input overdrive of 30 mV while consuming 7 µA. The block turns on immediately after the PV packet finishes transfer and, turns off as soon as t_{ON} goes low. The digital switches M_3, M_4, M_6, M_{13}, M_{14}, M_{16}, M_{18}, M_{19}, and M_{23} can disable the current paths to power gate the block when CP_{BA} is not in use.

5.1.2.5 Mode-Detect Comparator

The mode-detect comparator CP_M in Fig. 5.1, monitors v_O with respect to v_{REF} and sets the mode of operation for the system. In Fig. 5.7, the transconductance of M_3 and M_4 that operate near subthreshold produce current proportional to its transconductance. The positive feedback latch M_5, M_6, M_7 and M_8 takes these currents as input and latches the drain voltages of M_3 and M_4 depending on their initial state and the input current. For example with drain of M_3 near $v_{BAT,}$ when current in M_3 exceeds that in M_7, M_5 supplies the difference and M_6 mirrors it to charge the gate node of M_8 to turn off M_7 current, this way drain of M_3 comes down and M_4 goes to v_{BAT}.

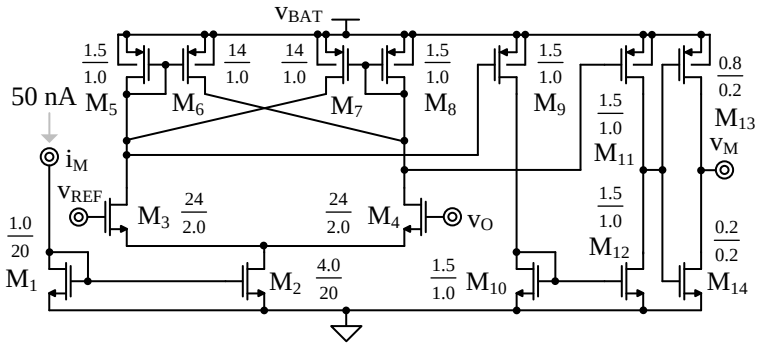


Fig. 5.7. Non-reversing mode-detect comparator.

The voltage difference between the gates of M_3 and M_4 that generate current to exceed M_6 and M_7 is around 75 mV, thus setting the symmetrical hysteresis window of the comparator at ±75 mV. The drain voltages of M3 and M4 set the current in M_9 and M_{11}.

At the drain of M_{11} and M_{12}, both currents compare to swing the signal to 0 or v_{BAT}. The M_{13}, M_{14} inverter further buffers the signal to the output v_M. The comparator consumes around 350 nA current and remains on all the to monitor v_O. The comparator has delay of less than 2 µs for an input overdrive of 5 mV. M_1–M_2 scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage.

5.1.2.6 Output-Diode Comparator

The output-diode comparator CP_O in Fig 5.1 measures voltage across the back to back switches M_{O1}–M_{O2} and turns off the switches when the voltage dips below zero. The two stage amplifier in Fig 5.8 in open loop implements the CP_O comparator. The transconductance gm_I of M_6 and M_7, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{SW} and v_O into a current. M_8–M_{19}, M_9–M_{10} and M_{14}–M_{16} mirror the current and, the output impedance of M_{16} and M_{19} translate the current to the single ended output that drives the gates of the inverter M_{23}–M_{24}. The inverter M_{25}–M_{26} inverters and buffers the signal to the output v_{DO}.

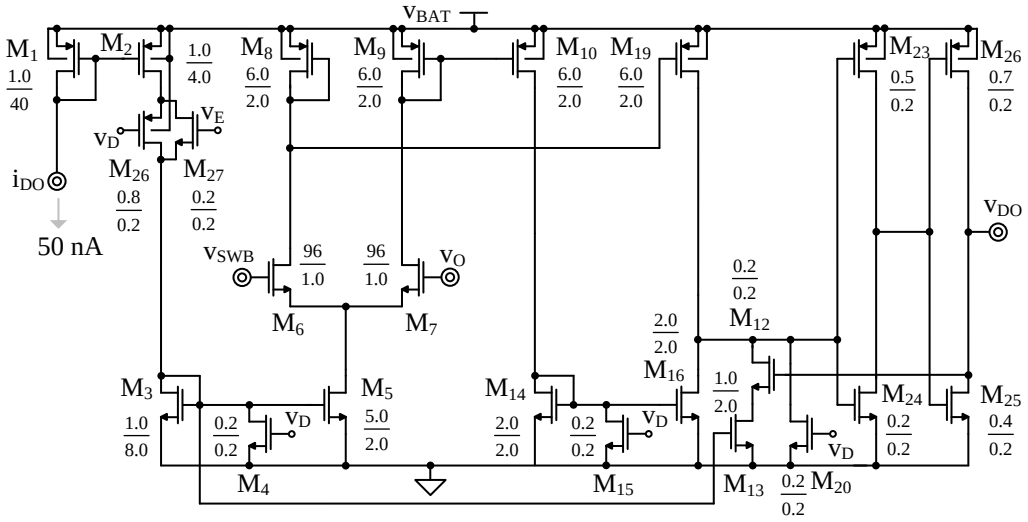


Fig. 5.8. Non-reversing output-diode comparator.

With the output of the inverter M_{23}–M_{24} low, M_{21} engages M_{22} to pull M_{23}–M_{24}'s gate high and reinforce the low state at its output. This way M_{22} sets a 5 mV hysteresis so that v_{DO} doesn't shuttle back and forth as the switch turns off. The comparator will detect zero crossing only after sufficient overdrive builds in the opposite direction, or in other words the switch current builds up sufficiently in the negative direction and thereby leading to larger losses. M_1–M_2 and M_3–M_5 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage.

The comparator has a delay of less than 40 ns for an input overdrive of 5 mV while consuming 15.5 µA current. The co-design of comparator and the respective switch can optimize the quiescent loss of the comparator with the ohmic loss of the switch to reduce the overall losses. The block turns on with low output state as soon as the switching node rises a diode above the battery voltage before the switch turns on and turns off as soon as the switch turns off. The digital switches M_4, M_{12}, M_{13}, M_{13}, M_{14}, M_{15}, M_{17}, M_{18}, M_{20}, M_{26} and M_{27} can disable the current paths to power gate the block in CP_O's off state.

5.1.2.7 Battery-Diode Comparator

The battery-diode comparator CP_B in Fig 5.1 measures voltage across the battery charging switches $M_{B(CHG)}$ turns off the switch when the voltage dips below zero. The two-stage current mode amplifier in Fig 5.12 in open loop implements the CP_B comparator. The transconductance gm_I of M_7 and M_{14}, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{SW} and v_{BAT} into a current. M_{10}–M_{18}, M_{11}–M_{23} and M_{15}–M_{20} mirror the current and, the output impedance of M_{20} and M_{23}

translate the current to the single ended output that drives the gates of the inverter M_{26}–M_{27}.

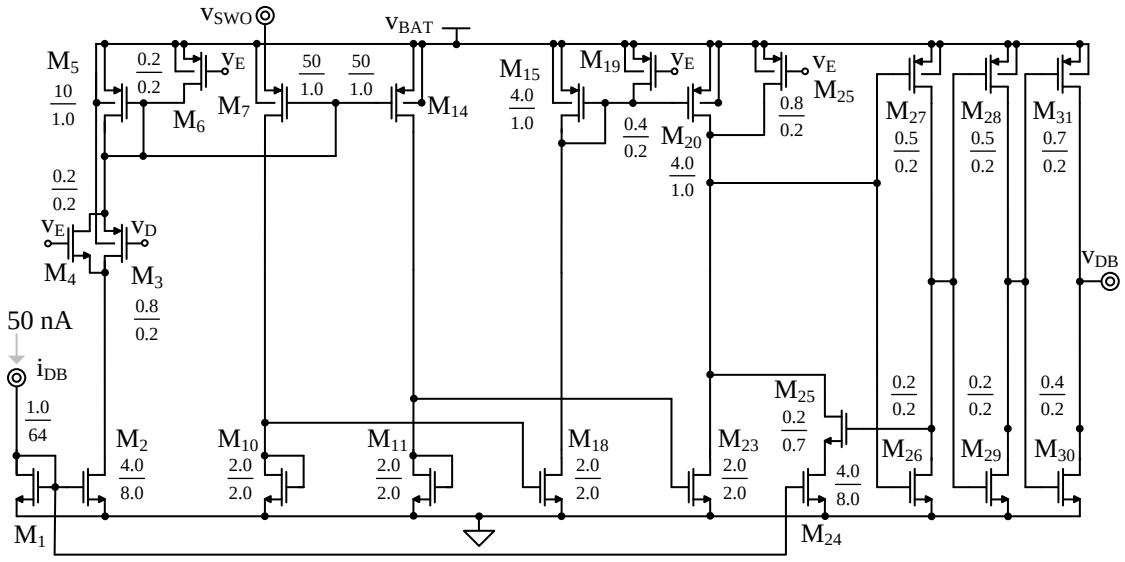


Fig. 5.9. Non-reversing battery-diode comparator.

The inverters M_{28}–M_{29} and M_{30}–M_{31} buffer the signal to the output v_{DB}. With the output of the inverter M_{26}–M_{27} high, M_{25} engages M_{24} to pull M_{26}–M_{27}'s gate low and reinforce the high state at its output. This way M_{24} sets a 5 mV hysteresis so that v_{DB} doesn't shuttle back and forth as the switch turns off. The comparator will detect zero crossing only after sufficient overdrive builds in the opposite direction, or in other words the switch current builds up sufficiently in the negative direction and thereby leading to larger losses. M_1–M_2 mirrors and scales the 50-nA bias current from the bias block to set the bias voltage at the gate of M_5 and gm_I of the input differential stage.

The comparator has a delay of less than 30 ns for an input overdrive of 5 mV while consuming 26 µA current. The co-design of comparator and the respective switch can optimize the quiescent loss of the comparator with the ohmic loss of the switch to

reduce the overall losses. The block turns on with low output state as soon as the switching node raises a diode above the battery voltage before the switch turns on and turns off as soon as the switch turns off. The digital switches M_3, M_4, M_6, M_8, M_9, M_{12}, M_{13}, M_{16}, M_{17}, M_{19}, M_{21}, M_{22} and M_{25} can disable the current paths to power gate the block in CP_B's off state.

5.1.2.8 Fixed On-Time Delays

The different delay blocks sets and limits the on-times of different power switches in the Fig. 5.1. Fig. 5.10 presents the circuit that implements the 500-µs mid PV packet sampling in Fig. 5.1. In Fig. 5.10 the M_5–M_6 charges capacitor C_{DLY} till its voltage cross trip point where M_{10}'s current exceeds M_{14}'s via switch M_{15}. After this trip point M_{11}'s source drops and increases M_{11}'s current to raise it above M_{13}'s and pulls the gate of M_{15}, M_{17} and M_{18} low. The inverters M_{19}–M_{20} and M_{21}–M_{22} buffer the signal, and set the output latch to set the output v_{DLO} high.

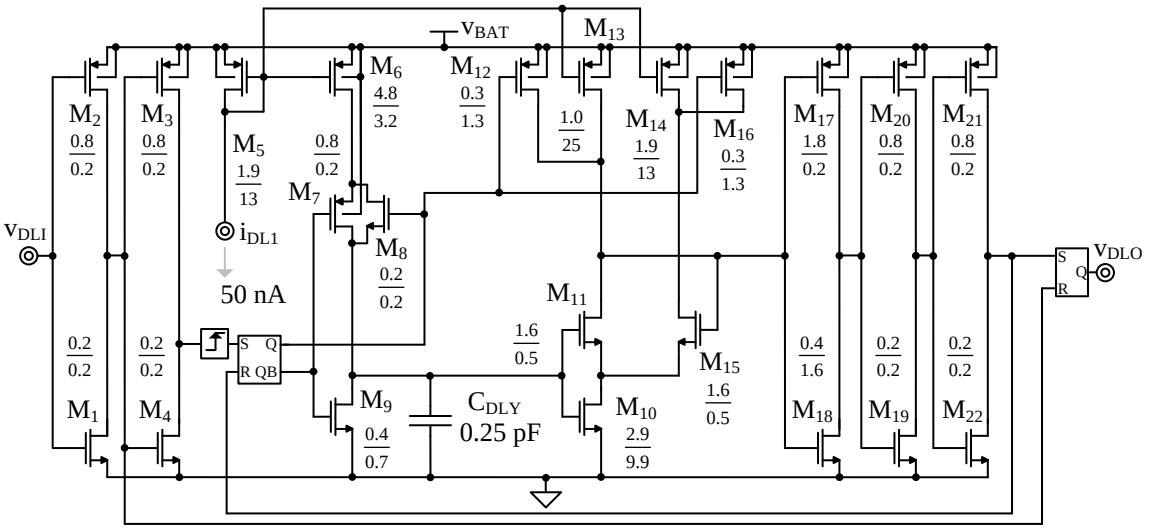


Fig. 5.10. Non-reversing fixed on-time delay.

The circuit engages at the rising edge of the input v_{DLI} through the inverters M_1–M_2 and M_3–M_4, the rising edge detector and the input SR latch. This way in Fig. 5.10 the output v_{DLO} turns high 500 µs after v_{DLI} turns high and turns low immediately as v_{DLI} turns low through the resetting of the output SR latch. The digital switches M_7, M_8, M_{12} and M_{16} turns off and power gates the delay block when not in use.

5.1.2.9 PTAT Bias Current Generator

The proportional to absolute temperature (PTAT) bias current generator in Fig. 5.15 generates and supplies the bias currents for all the comparators and amplifiers in the system. For this, M_4 and the 8 times bigger M_5 apply the difference in gate source voltage around 60 mV across an external 1.2 MΩ resistor to generate a 50 nA current. As the transistors operate in subthreshold, the difference in the gate source voltages has a proportional to temperature coefficient. The PTAT current increases with temperature and ensure the bias currents that run the comparator scale and dominate as transistor leakage currents increase with temperature.

The transistor M_4, M_5, M_6, M_7, M_8 and M_9 form a positive feedback loop that latches the current at a stable operating point of 50 nA. However, zero current condition is also a stable operating point, and M_1, M_2 and M_3 form a startup circuit to pull the circuit out of zero current state. When M_4 and M_5 conduct zero current M_2 is off and M_1 pulls the gate of M_3 high, M_3 turns on to leak current from the gate of M_9 and M_8 to push the latch away from zero current. At the desirable operating point M_2 conducts enough current to turn off M_3. The transistors M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16} mirrors the 50 nA bias current bias the different blocks. Overall the always on bias block consumes about 350 nA through its various legs. Reducing the magnitude of the single leg current

below 50 nA can reduce the quiescent losses and improve the low power efficiency of the system, however this can make the circuits sensitive to the substrate noise.

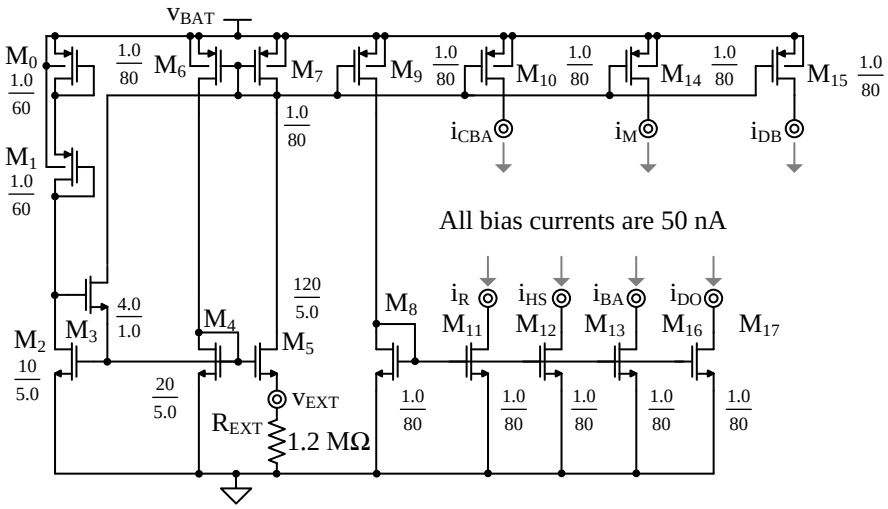


Fig. 5.11. Non-reversing PTAT bias current generator.

5.1.3 Power Switches

Power switch design balances the ohmic loss, gate-drive loss and controller losses as Chapter3 shows. The switching logic in Fig. 5.1 generates the on and off signal that the switch drivers buffer and propagate to turn on and off the switches. Driving the gate of large switch with a minimum size inverter can lead to slow transition of the gate signal and large turn on time and shoot through losses. Therefore switch drivers consists of a chain series of inverter with each successive stage 5× to 7× times the previous driving inverter in the chain. This way, the gate-drive signal propagates with minimum delay and incurs minimum shoot-through loss in each inverter stage. The remaining sections present the switch size and the switch driving logic for the switches in Fig. 5.1. In the non-reversing switching circuit of Fig. 5.1 M_{PV}, M_{G2} and M_{O1}–M_{O2} and $M_{B(CHG)}$ transfers 10–100 µW photovoltaic power to the output and $M_{B(AID)}$, M_{G1} and M_{O1}–M_{O2} transfers up to

1 mW battery power to the output. The circuit scales the frequency of PV packets with P_{PV} and size of the battery packet with P_{LD}.

5.1.3.1 Photovoltaic Ground Switch

Design: The photovoltaic ground switch engages during the energizing time t_{PE} of the photovoltaic energy packet E_{PV} of Fig. 4.3. During the on time of the switch, the switch current which is same as the inductor current rises from zero to 5 mA in 1 µs. The switch is NMOS as the NMOS conducts ground voltages more efficiently and the body diode of the switch provides dead time current path for the inductor current flows out of the v_{SWO} node in Fig. 5.1. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch 1020 µm, in Fig. 5.12, balances both the ohmic and switching losses and presents a series resistance of 0.5 Ω. As only the frequency of the constant size PV packet varies with photovoltaic power P_{PV}, both the ohmic losses and switching losses scale with P_{PV} and as a result a single switch size is optimum across P_{PV}.

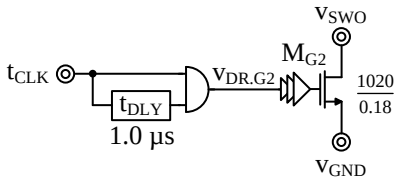


Fig. 5.12. Non-reversing photovoltaic ground switch and driving logic.

Switching Logic: In the non-reversing circuit of Fig 5.1 the energizing time of the photovoltaic packet is 1 µs. To implement this in Fig. 5.12 an external clock t_{CLK} sets the frequency of the PV packets and changes according to the light level from 8 kHz at 10 µW P_{PV} to 90 kHz for 100 µW P_{PV}. To generate the 1 µs on-time energizing pulse at

every rising edge of the clock, the logic circuit in Fig. 5.12, delays t_{CLK} and an AND gate combines the t_{CLK} and the delayed-t_{CLK} to generate $v_{DR.G2}$ that drives the gate-driving buffer to switch M_{G2} and off.

5.1.3.2 Photovoltaic Switch

Design: The photovoltaic switch engages for the entire duration in heavily-sourced mode and for the duration of the PV packet transfer in battery-assisted mode. During the on time of the switch, the switch current which is same as the inductor PV-packet current rises from zero to 5 mA in 1 µs and drops from 5 mA back to zero in 425 ns while supplying output and 200ns while charging battery, Fig. 4.1 and Fig. 4.3. The switch is NMOS as the NMOS conducts low voltages more efficiently and the photovoltaic voltage is only around 0.3 V. The body diode of the switch provides dead time current path for the inductor current flows out of the v_{SWP} node in Fig. 5.1. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch 1520 µm, in Fig. 5.13, balances both the ohmic and switching losses and presents a series resistance of 0.45 Ω in the battery-assist mode.

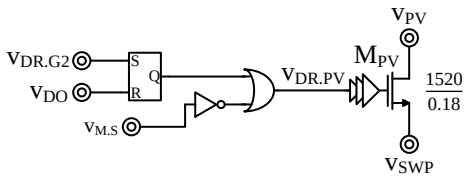


Fig. 5.13. Non-reversing photovoltaic switch and driving logic.

The source of M_{PV} connects to v_{PV} of 0.3 V as a result the on-time gate source voltage is lower than that of M_{G2}, therefore resistance only changes by 50 mΩ even for

1.5 times increase in area. As only the frequency of the constant size PV packet varies with photovoltaic power P_{PV}, both the ohmic losses and switching losses scale with P_{PV} and as a result a single switch size is optimum across P_{PV} in battery-assist mode. However in case of heavily-sourced mode the switch engages during the entire duration and as a result the ohmic losses dominate in this mode.

Switching Logic: The signals that determine the driving signal for M_{PV} are the sampled mode-detect comparator output $v_{M.S}$, the driving signal $v_{DR.G2}$ of the switch M_{G2} and the output diode comparator output v_{DO}. To generate the $v_{M.S}$ a latch samples the output v_M of the mode comparator midway of PV packet's energizing time. The digital circuit in Fig. 5.13 implements the driving logic for M_{PV} switch. In heavily-sourced mode $v_{M.S}$ turns low and driving $v_{DR.PV}$ high via inverter and OR gate for the entire during of the heavily sourced mode. In battery-assisted mode a SR latch drives $v_{DR.PV}$, the SR latch turns high as soon as the M_{G2} engages via $v_{DR.G2}$ and turns off as PV packet finishes via v_{DO}.

5.1.3.3 Output Switch

Design: The output switch M_{O1}–M_{O2} engages for the de-energizing time of the PV packet that supplies the load and, during the transfer of the entire battery packet. In heavily sourced mode the circuit only transfers the PV packets and they reach the output as is it drops a threshold below reference thereby by tripping CP_{HS}. In this mode during the on time of the switch, the switch current quickly rises to the inductor peak current of 5 mA as it turns on and flows it till the current drops to zero thereby tripping CP_O and turning off the switch. Typically on time of the switch in this mode is 425 ns. In the battery-assist

mode the switch remains on for the entire duration of the battery packet in addition to the de-energizing time of the PV packet. Typically the on time of the switch in this mode is around 1.5 µs for 500 µW P_{LD}.

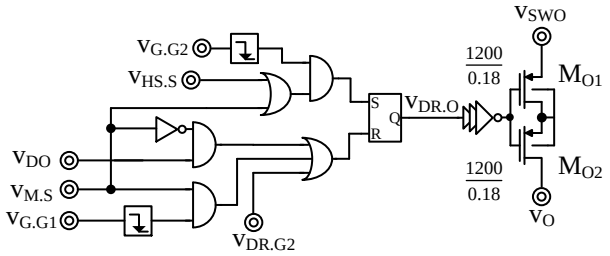


Fig. 5.14. Non-reversing output switch and driving logic.

The switch that implements the output switch is a back-back PMOS as the PMOS conducts high voltages more efficiently and the back-back body diodes block current flow when the circuit charges battery and as a result the switching node rises to v_{BAT}. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of each switch at 1200 µm, in Fig. 5.14, balances both the ohmic, gate-drive loss and the quiescent power of the comparator across it. The switch presents a series resistance of around 6 Ω, this is leads to high ohmic losses but gives enough overdrive for the comparator to drip faster when the current drops to zero. Adding an offset to the comparator can allow the switch to scale larger and better efficiency. As only the frequency of the constant size PV packet varies with photovoltaic power P_{PV}, both the ohmic losses and switching losses scale with P_{PV} in heavily sourced mode, however in battery-assist mode the switch engages during the entire duration of the battery packet

with the ohmic losses scaling quadratically and the battery power linearly with load power. As a result the ohmic losses dominate as the power increases and efficiency drops.

Switching Logic: The signals that determine the gate driving signal $v_{DR.O}$ of M_{O1}–M_{O2} are the gate drive signal $v_{DR.G2}$ and gate signal $v_{G.G2}$ of switch M_{G2}, the gate signal $v_{G.G1}$ of switch M_{G1}, the sampled output of heavily source comparator $v_{HS.S}$, $v_{M.S}$, and v_{DO}. To generate the $v_{HS.S}$ a latch samples the output v_{HS} of the heavily source comparator midway of PV packet's energizing time. The digital circuit in Fig. 5.14 implements the driving logic for M_{O1}–M_{O2} switch. In Fig. 5.14 the falling edge of the $v_{G.G2}$ sets the SR latch that drive $v_{DR.O}$ in battery assist mode and only when $v_{HS.S}$ is high in heavily sourced mode. In heavily sourced mode v_{DO} and in battery assist mode the falling edge of $v_{G.G1}$ resets the SR latch and $v_{DR.O}$. The high state of $v_{DR.G2}$ resets the output switch to prevent shorting of the output in case of faults.

5.1.3.4 Battery Charge Switch

Design: The battery charge switch $M_{B(CHG)}$ switch engages for the de-energizing time of the PV packet that charges the battery in the heavily sourced mode. In this mode during the on time of the switch, the switch current quickly rises to the inductor peak current of 5 mA as it turns on and flows it till the current drops to zero thereby tripping CP_B and turning off the switch. Typically on time of the switch in this mode is 200 ns. The switch that implements $M_{B(CHG)}$ is a PMOS switch in Fig.5.15 as the PMOS conducts high voltages more efficiently and the body diode of the switch provides dead time current path for the inductor current flows into the v_{SWO} node in Fig. 5.1.

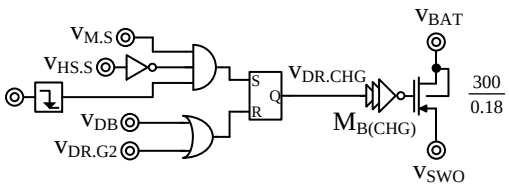


Fig. 5.15. Non-reversing battery charge switch and driving logic.

The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch at 300 µm, in Fig. 5.15, balances both the ohmic, gate-drive loss and the quiescent power of the comparator across it. The switch presents a series resistance of around 7.5 Ω, this leads to high ohmic losses but gives enough overdrive for the comparator to drip faster when the current drops to zero. Adding an offset to the comparator can allow the switch to scale larger and better efficiency. As only the frequency of the constant size PV packet varies with photovoltaic power P_{PV}, both the ohmic losses and switching losses scale with P_{PV} in heavily sourced mode.

Switching Logic: The signals that determine the gate driving signal $v_{DR.CHG}$ of $M_{B(CHG)}$ are the gate drive signal $v_{DR.G2}$ and gate signal $v_{G.G2}$ of switch M_{G2}, the output of battery diode comparator v_{DB}, $v_{HS.S}$, and $v_{M.S}$. The digital circuit in Fig. 5.15 implements the driving logic for $M_{B(CHG)}$ switch. In Fig 5.15 the falling edge of the $v_{G.G2}$ sets the SR latch that drive $v_{DR.CHG}$ only when $v_{HS.S}$ is low in heavily sourced mode. In heavily sourced mode v_{DB} resets the SR latch and $v_{DR.O}$. The high state of $v_{DR.G2}$ resets the battery charge switch to prevent shorting of the battery in case of faults.

5.1.3.5 Battery-Assist Switch

Design: The battery assist switch $M_{B(AID)}$ switch engages during for the energizing time of the battery packet in the battery-assist mode. In this mode during the on time of the switch, the switch current rises from zero to the battery packet peak current. In circuit of Fig. 5.1 the size of battery packet depends on the load requirement. For instance the for a load power of 500 µW, the switch on time is around 700 ns and the inductor current rises from 0 to 12 mA. The battery assist comparator CP_{BA} compares v_{EA} and v_R to set the battery packet energizing time.

The switch that implements $M_{B(AID)}$ is a PMOS switch in Fig. 5.16 as the PMOS conducts high voltages more efficiently and the body diode of the switch provides dead time current path for the inductor current that flows into the v_{SWP} node in Fig. 5.1. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch at 6000 µm, in Fig. 5.16, balances both the ohmic, gate-drive loss for the mid-range load power of 500 µW. The switch presents a series resistance of around 0.38 Ω, this leads to high ohmic losses at higher power levels and higher switching losses for power level lower than 500 µW. In battery-assist mode the switch engages during the duration of the battery packet energizing time with the ohmic losses scaling quadratically and the battery power linearly with load power. As a result the ohmic losses dominate as the power increases and efficiency drops.

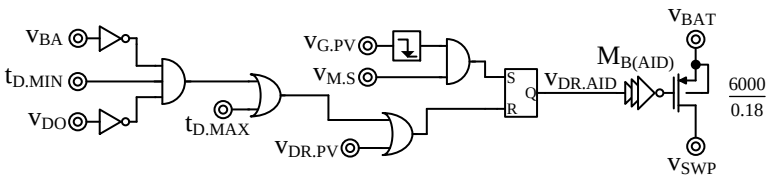


Fig. 5.16. Non-reversing battery-assist switch and driving logic.

Switching Logic: The signals that determine the gate driving signal $v_{DR.AID}$ of $M_{B(AID)}$ are the gate drive signal $v_{DR.PV}$, the PV switch gate signal $v_{G.PV}$, the minimum battery energizing time pulse $t_{D.MIN}$, the maximum battery energizing time pulse $t_{D(MAX)}$, the output v_{BA} of CP_{BA}, v_{DO} and $v_{M.S}$. The digital circuit in Fig. 5.16 implements the driving logic for $M_{B(AID)}$ switch. In Fig 5.16 the falling edge of the $v_{G.PV}$ sets the SR latch that drive $v_{DR.CHG}$ only in the battery assist mode. The reset signal turns high when v_{BA} turns low between the battery energizing time $t_{D(MIN)}$ and $t_{D(MAX)}$. This way the switch remains on for a duration between $t_{D(MIN)}$ and $t_{D(MAX)}$.The high state of $v_{DR.PV}$ resets the battery aid switch to prevent shorting of the battery in case of faults.

5.1.3.6 Battery-Assist Ground Switch

Design: The battery-assist switch M_{G1} switch engages during the de-energizing time of the battery packet in the battery-assist mode. In this mode as the switch turns on the switch current quickly rises to the battery packet peak current, during the on time of the switch, the switch current falls from peak current to zero. In circuit of Fig. 5.1 the size of battery packet and the de-energizing time depends on the load requirement. For instance at a load power of 500 μW, the switch on time is around 560 ns and the inductor current falls from 12 mA to 0.

The switch that implements M_{G1} is a NMOS switch in Fig. 5.17 as the NMOS conducts ground voltages more efficiently and the body diode of the switch provides dead time current path for the inductor current that flows out of the v_{SWP} node in Fig. 5.1. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch at 2520 µm, in Fig. 5.17, balances both the ohmic, gate-drive loss for the mid-range load power of 500 µW. The switch presents a series resistance of around 0.2 **Ω**, this leads to high ohmic losses at higher power levels and higher switching losses for power level lower than 500 µW. In battery-assist mode the switch engages during the duration of the battery packet de-energizing time with the ohmic losses scaling quadratically and the battery power linearly with load power. As a result the ohmic losses dominate as the power increases and efficiency drops.

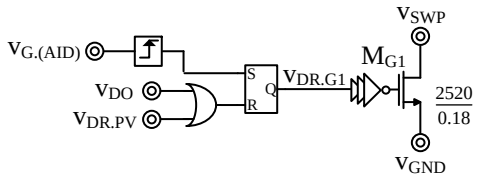


Fig. 5.17. Non-reversing battery-assist ground switch and driving logic.

Switching Logic: The signals that determine the gate driving signal $v_{DR.G1}$ of M_{G1} are the gate drive signal $v_{DR.PV}$, the battery assist switch gate signal $v_{G.(AID)}$ and, v_{DO}. The digital circuit in Fig. 5.17 implements the driving logic for M_{G1} switch. In Fig 5.17 the rising edge of the $v_{G.(AID)}$ sets the SR latch that drive $v_{DR.G1}$ and v_{DO} resets the latch to turn on and off the switch driving signal $v_{DR.G1}$. The high state of $v_{DR.PV}$ resets the battery aid switch to prevent shorting of the battery in case of faults.

5.2 Reversing CMOS Charger–Supply

5.2.1 System

The photovoltaic switch M_{PV}, the ground switch M_G, the photovoltaic switch M_{SUP1}–M_{SUP2}, the battery switch M_B and the battery-assist output switch $M_{O(AID)}$ implements the reversing power stage in Fig. 5.18. M_{PV} and M_G close to energize the inductor L_X from photovoltaic voltage v_{PV} to ground. M_{SUP1}–M_{OUP2} and M_{PV} close to drain the inductor from v_{PV} to output v_O, thereby supplying photovoltaic power to v_O. Similarly M_{PV} and M_B close to drain L_X from v_{PV} to battery v_{BAT}, and charge the battery with excess photovoltaic power. $M_{O(AID)}$ and M_B close to energize L_X from v_{BAT} to v_O. $M_{O(AID)}$ and M_G can close to drain the remaining battery energy to v_O. For higher efficiency at low power levels the circuit operates in DCM, M_{NR} is the ring kill switch engages when all the switches close to dissipate remnant inductor energy after power transfers.

The power stage in Fig. 5.18 engages different switch sizes depending on the mode of power and as a result different power transfer levels and losses. For example in the heavily sourced mode M_{PV} is on all the time and as a result the entire switch engages , but in battery-assist mode the M_{PV} needs to disengage after every PV packet and as a result the only part of the switch engages to reduce the switching losses of a large switch. Similarly the battery and ground switch carry larges energy packets and as a result more power and engages fully in battery-assist mode to reduce the losses.

The control blocks in Fig. 5.18 processes voltages and currents and along with the logic block generates switching signals for the power stage. The major blocks in the design, in Fig. 5.18, are error amplifier G_{BA}, battery-assist comparator CP_{BA}, heavily source

comparator CP_{HS}, mode-detect comparator CP_M and the diode comparators CP_O, CP_G and CP_B. CP_O, CP_G and CP_B are diode comparators that digital logic can enable to measure voltage across switches $M_{O(SUP)1}$–$M_{O(SUP)2}$, M_G and M_B turn of the respective switches when inductor depletes.

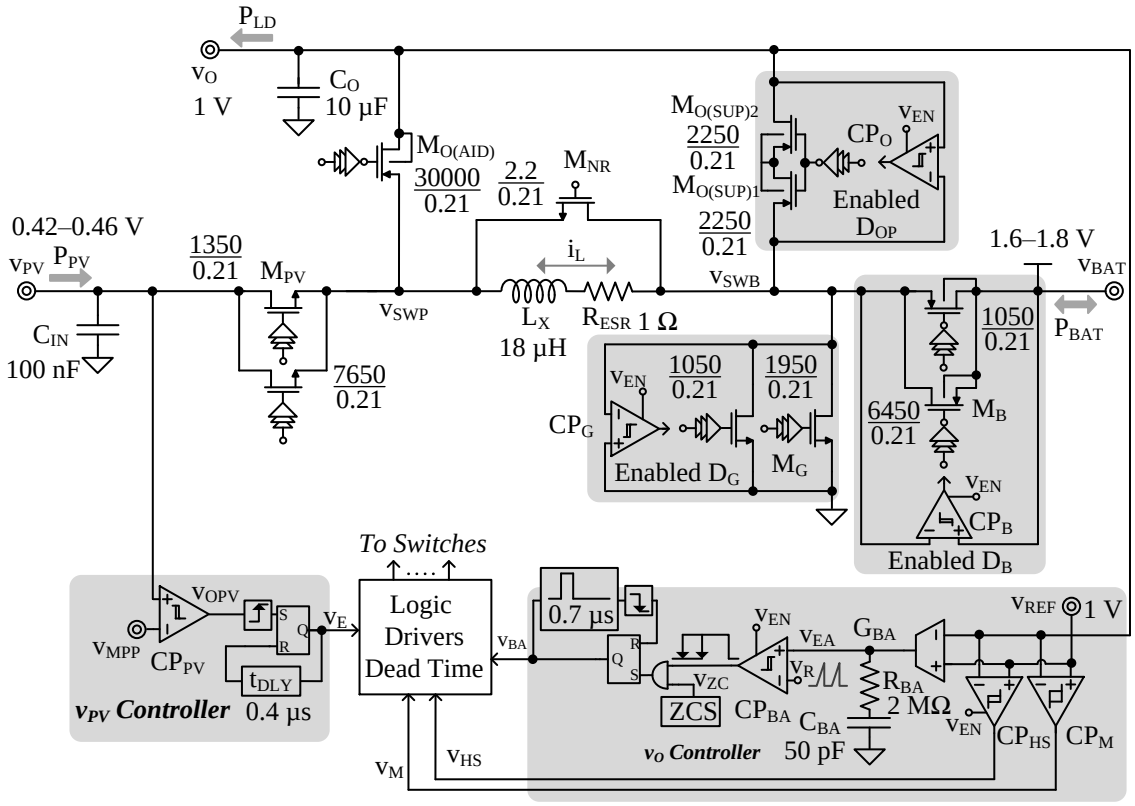


Fig. 5.18. Reversing switched-inductor charger–supply CMOS implementation.

CP_{HS} is the inner hysteretic comparator that compares v_O and the reference voltage v_{REF} to determine the direction of energy flow in heavily-sourced mode. The battery-assist transconductor G_{BA} amplifies the difference between v_O and v_{REF} that the filter R_{BA}-C_{BA} filters to generate error voltage v_{EA}. The battery-assist comparator CP_{BA} compares v_{EA} and the ramp signal v_R to generate the on-time signal v_{ON} for battery packets. Further the SR latch and 0.7-µs delay generates constant energizing battery

packets for the duration of v_{ON}. Unlike the non-reversing case CP_{PV} compares v_{PV} with v_{MPP} to trigger the onset of the PV packet and the fixed 0.4-µs delay block sets the energizing time of the PV packet.

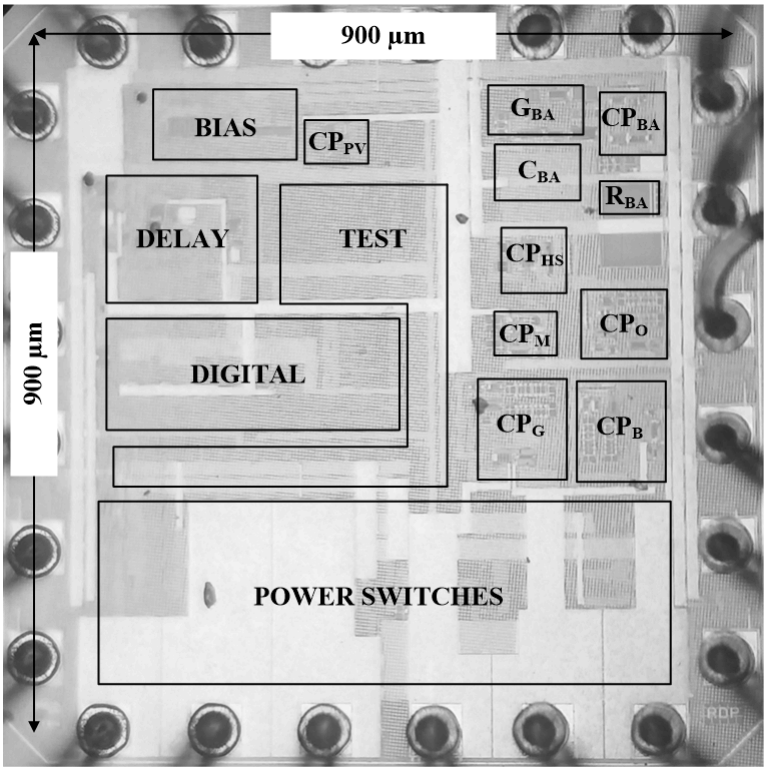


Fig. 5.19. Reversing switched-inductor charger–supply die photograph.

The 0.18-µm CMOS non-reversing variable size battery packet integrated circuit (IC) along with the test circuitry occupies 900 × 900 μm^2 in Fig. 5.19. This system transfers between 10–130 µW photovoltaic power and remaining battery power to supply upto 10-mW load and charge battery with extra PV power. The power switches occupy about 20% of the IC. as in the non-reversing circuit the location of the switches, pins and the orientation of the metal connections to drain and source are important considerations that reduce the series path resistance. The major considerations that determine the placement of the control block are noise sensitivity, interconnects supply routing. The

placement of the diode comparators CP_B and CP_G are close to the switches as they are current mode comparators that draw current from the measure voltage nodes. CP_O can be further away as it is common source input comparator that doesn't draw current from the input nodes. The comparators and capacitors shield the noise sensitive error amplifier and bias block from the digital noise. The delay block occupies a lot space due to the large area capacitors scaling down the charging current can reduce the capacitor size at the cost of higher noise sensitivity.

5.2.2 Controller Circuits

5.2.2.1 Photovoltaic_Comparator

The PV loop comparator, CP_{PV} in Fig. 5.18 compares v_{PV} with v_{MPP} to regulate v_{PV} about the maximum power point $v_{PV(MPP)}$. The two stage amplifier in Fig 5.20 in open loop implements the CP_{PV} comparator. The transconductance gm_I of M_3 and M_4, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{PV} and v_{MPP} into a current, M_5 and M_6 mirrors the current and, the output impedance of M_4 and M_6 translate the current to the single ended output that drives the gate of M_9. M_9 and M_{10} further amplify the signal to full swing of 0 to v_{BAT}. The inverters M_{11}, M_{12} and M_{13}, M_{43} buffer the signal to the output v_{OPV}.

With v_{OPV} high, M_8 engages M_7 to further pull M_9's gate low and reinforce v_{OPV} high state. This way M_7 sets a 3 mV hysteresis so that v_{OPV} doesn't shuttle back and forth with noise at v_{PV} around $v_{MPP.}$ M_1 and M_2 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage. The

comparator has a delay of less than 2 μs for an input overdrive of 5 mV. As CP_{PV} needs to continually monitor v_{PV} it remains on all the time, and consumes 300 nA current.

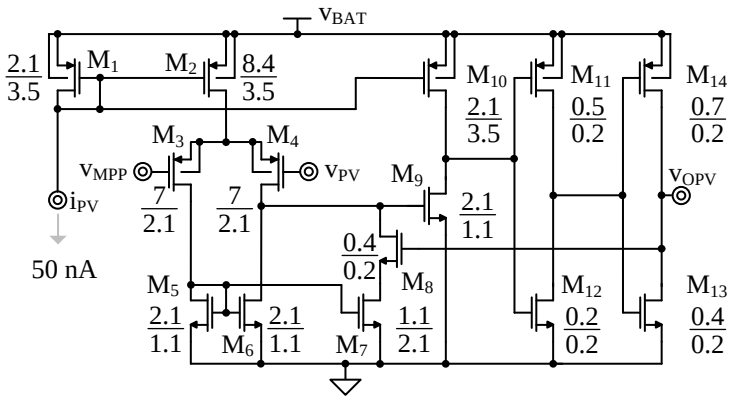


Fig. 5.20. Reversing photovoltaic comparator.

5.2.2.2 Heavily Sourced Comparator

The heavily sourced comparator CP_{HS} in Fig. 5.18 monitors v_O and regulates it around v_{REF}. As in the case of $CP_{PV,}$ a two stage amplifier in open loop implements the comparator in Fig. 5.21. The transconductance of M_8 and M_9 that operate near subthreshold amplifies the voltage difference between v_{REF} and v_O into a current, M_{10} and M_{12} mirrors the current and, the output impedance of M_9 and M_{12} translate the current to a single ended output that drives the gate of M_{16}. M_{16} and M_{17} further amplify the signal to full swing of 0 to v_{BAT}. The inverter M_{18} and M_{19} buffers the signal to the output v_{HS}.

v_{OSB} that drive the gate of M_{14} is a latched and inverted version of v_{HS}. When v_{OSB} is low M_{15} adds an additional current that input overdrive has to overcome to flip v_{HS}, and thereby implements the hysteresis. Further M_9 is bigger than M_8 to add an offset that centers the hysteresis about v_{REF}. This way the v_{HS} trips low when vo rises 28 mV above v_{REF} and trips high when v_O falls 28 mV below v_{REF}. The digital switches M_3, M_4, M_6,

M_{11} and M_{13} can disable the current paths to power gate the block when CP_{HS} is not in use.

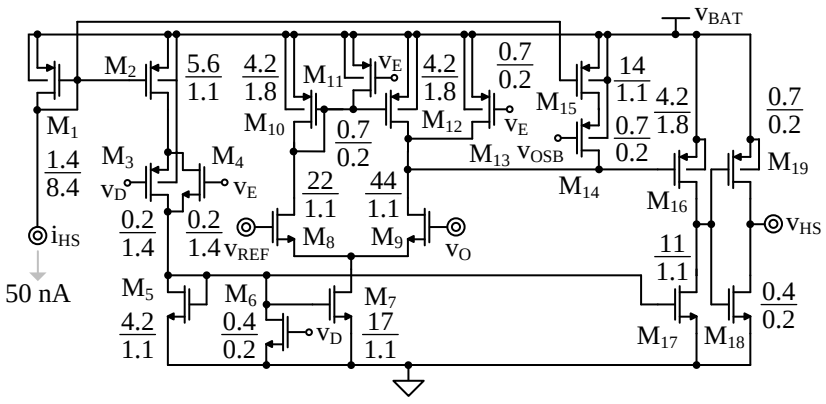


Fig. 5.21. Reversing heavily sourced comparator.

The comparator turns on only in the HS mode during the energizing time of E_{PV}, makes the decision on the direction to send E_{PV} and then turns off. The digital logic samples and latches v_{HS} before it turns off and retains v_{HS} when CP_{HS} turns back on via v_{OSB}. M_1, M_2, M_5 and M_7 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage. The comparator consumes around 12 µA current when it is on. As the comparator needs to make a decision mid-way through the E_{PV} energizing time of 400 ns it has a delay of less than 150 ns for 2 mV overdrive.

5.2.2.3 Battery-Assist Transconductor

The battery-assist transconductor G_{BA} in Fig. 5.18 amplifies the voltage difference between v_O and v_{REF} to output v_{EA}. The folded cascade amplifier in Fig. 5.22 implements G_{BA}. The transconductance of M_8 and M_9 that operate near subthreshold amplifies the voltage difference v_O and v_{REF} into a current. M_{17} and M_{23} set the fixed-bias currents in

the output legs. M_{18} and M_{15} sink the current difference that M_8 and M_9 generates. M_{16} and M_{17} mirror the current difference to the output node v_{EA}. The output impedance of the long FET M_{21} and the cascode of M_{22} and M_{23} translate the current to the single ended output v_{EA}. M_1, M_2, M_5 and M_7 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage. M_{10}, M_{11}, M_{13}, M_{14} and M_{15} generate the biasing voltages for the cascade transistors.

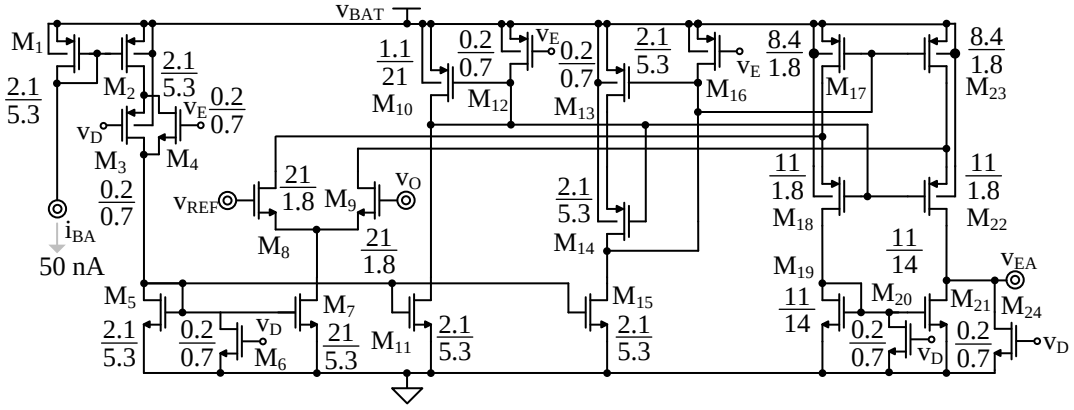


Fig. 5.22. Reversing battery-assist transconductor.

The digital switches M_3, M_4, M_6, M_{12}, M_{16} and M_{20} can disable the current paths to power gate the block when G_{BA} not in use. The transconductor block turns on only during battery-assistance mode. For the reversing circuit a 50 pF internal capacitance and 2 MΩ internal resistor implements the compensation, and as a result the output impedance of G_{BA} in Fig. 5.18 and Fig. 5.22 is higher at 100 MΩ and the gain across all temperature and process corners is higher than 60 dB.

5.2.2.4 Ramp Generator

To generate the ramp signal the ramp generator circuit in Fig. 5.23 charges a capacitor with a constant current. In Fig 5.18 the ramp generator circuit turns on at the

end of the PV packet. M_1 and M_2 mirrors the 50 nA bias current i_R to charge the capacitor voltage v_R as soon as the circuit turns on. The diode connected transistor M_5 adds an offset to v_R so that minimum v_R value and as a result the corresponding v_{EA} is high enough to reduce noise susceptibility. The lowest photovoltaic frequency and the input common mode range of the battery-assist comparator determine the ramp rate. The digital switches M_3 and M_4 can disable the current path to power gate the block the ramp generator.

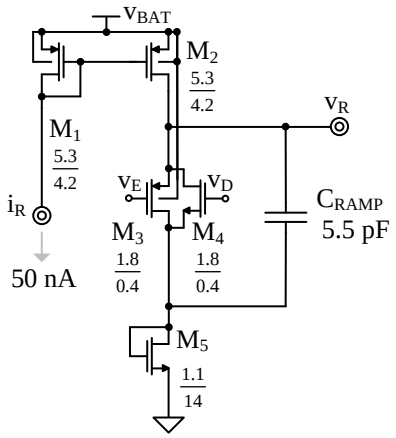


Fig. 5.23. Reversing ramp generator.

5.2.2.5 Battery-Assist Comparator

The battery-assist comparator CP_{BA} in Fig 5.18 compares the error voltage v_{EA} and ramp signal v_R to set the energizing time for variable size battery packet or the on-time for the multiple packet case. The two stage amplifier in Fig 5.24 in open loop implements the CP_{BA} comparator. The transconductance gm_I of M_8 and M_9, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{EA} and v_R into a current. M_{10}–M_{12}, M_{11}–M_{20} and M_{15}–M_{17} mirrors the current and, the output impedance of M_{17} and M_{20} translate the current to the single ended output that drives the gates of the

inverter M_{24}–M_{25}. The inverters M_{26}–M_{27} and M_{28}–M_{29} buffer the signal to the output v_{ON}.

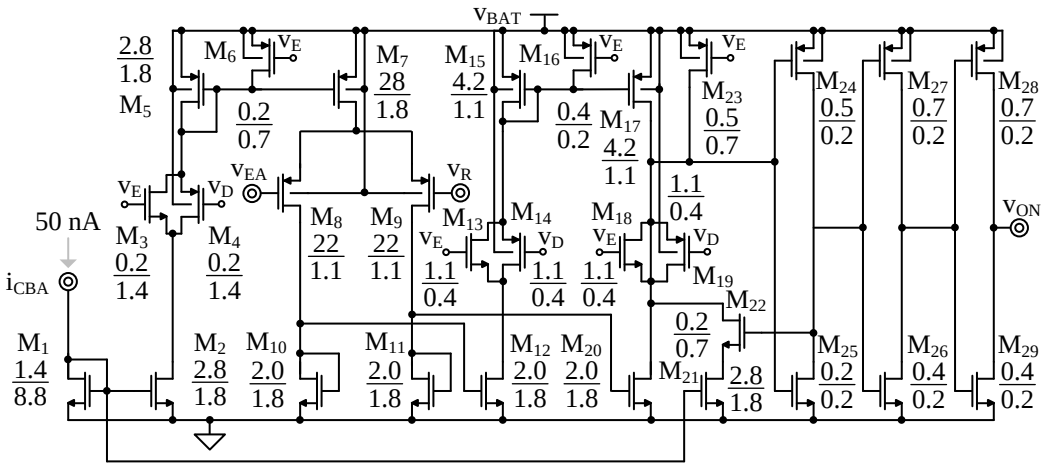


Fig. 5.24. Reversing battery-assist comparator.

With the output of the inverter M_{24}–M_{25} high, M_{22} engages M_{21} to further pull M_{24}–M_{25}'s gate low and reinforce the high state at its output. This way M_{21} sets a 5 mV hysteresis so that v_{ON} doesn't shuttle back and forth with noise at v_R or v_{EA} around the trip point. M_1–M_2 and M_6–M_7 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage. The comparator has a delay of less than 200 ns for an input overdrive of 5 mV while consuming. The block turns on immediately after the PV packet finishes transfer and, turns off as soon as t_{ON} goes low. The digital switches M_3, M_4, M_6, M_{13}, M_{14}, M_{16}, M_{18}, M_{19}, and M_{23} can disable the current paths to power gate the block when CP_{BA} is not in use.

5.2.2.6 Mode-Detect Comparator

The mode-detect comparator CP_M in Fig. 5.18, monitors v_O with respect to v_{REF} and sets the mode of operation for the system. In Fig. 5.25, the transconductance of M_3

and M_4 that operate near subthreshold produce current proportional to its transconductance. The positive feedback latch M_5, M_6, M_7 and M_8 takes these currents as input and latches the drain voltages of M_3 and M_4 depending on their initial state and the input current. For example with drain of M_3 near $v_{BAT,}$ when current in M_3 exceeds that in M_7, M_5 supplies the difference and M_6 mirrors it to charge the gate node of M_8 to turn off M_7 current, this way drain of M_3 comes down and M_4 goes to v_{BAT}. The voltage difference between the gates of M_3 and M_4 that generate current to exceed M_6 and M_7 is around 60 mV, thus setting the symmetrical hysteresis window of the comparator at ± 60 mV. The drain voltages of M3 and M4 set the current in M_9 and M_{11}. At the drain of M_{11} and M_{12}, both currents compare to swing the signal to 0 or v_{BAT}. The M_{13}, M_{14} inverter further buffers the signal to the output v_M. The comparator consumes around 350 nA current and remains on all the to monitor v_O. The comparator has delay of less than 2 µs for an input overdrive of 5 mV. M_1–M_2 scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage.

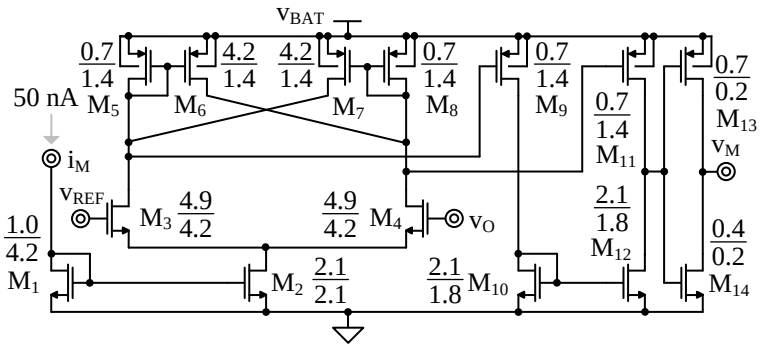


Fig. 5.25. Reversing mode-detect comparator.

5.2.2.7 Output-Diode Comparator

The output-diode comparator CP_O in Fig. 5.18 measures voltage across the back to back switches M_{O1}–M_{O2} and $M_{O(SUP)1}$–$M_{O(SUP)2}$ respectively and turns off the switches when the voltage dips below zero. The two stage amplifier in Fig 5.26 in open loop implements the CP_O comparator. The transconductance gm_I of M_6 and M_7, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{SW} and v_O into a current. M_8–M_{19}, M_9–M_{10} and M_{14}–M_{16} mirror the current and, the output impedance of M_{16} and M_{19} translate the current to the single ended output that drives the gates of the inverter M_{23}–M_{24}. The inverter M_{25}–M_{26} inverters and buffers the signal to the output v_{DO}.

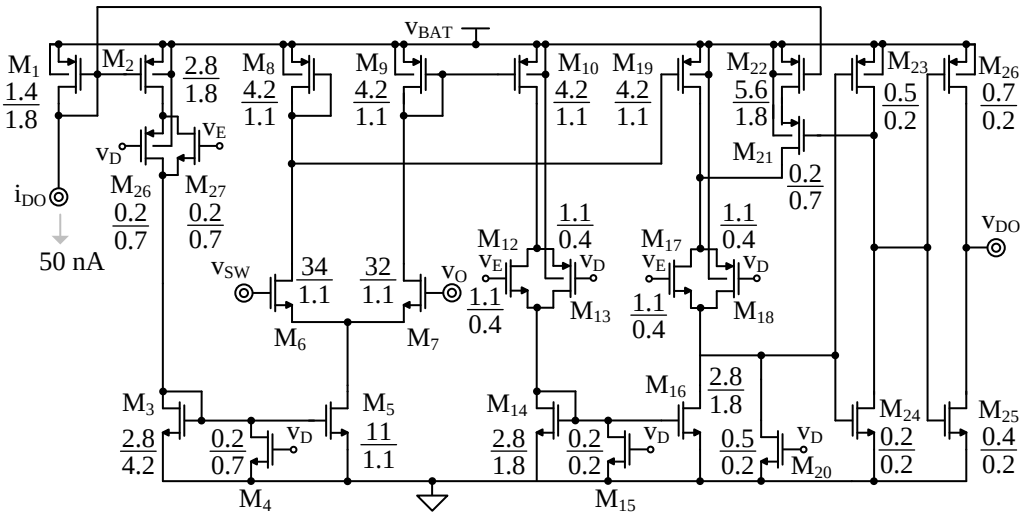


Fig. 5.26. Reversing output-diode comparator.

With the output of the inverter M_{23}–M_{24} low, M_{21} engages M_{22} to pull M_{23}–M_{24}'s gate high and reinforce the low state at its output. This way M_{22} sets a 5 mV hysteresis so that v_{DO} doesn't shuttle back and forth as the switch turns off. The difference in size between M_6 and M_7 introduces a slight offset to aid the comparator switch state exactly at

the zero crossing point of the switch voltage, in Fig. 5.18. In the absence of the offset Fig. 5.1 the comparator will detect zero crossing only after sufficient overdrive builds in the opposite direction, or in other words the switch current builds up sufficiently in the negative direction and thereby leading to larger losses. M_1–M_2 and M_3–M_5 mirrors and scales the 50-nA bias current from the bias block to set the tail current and gm_I of the input differential stage.

The comparator has a delay of less than 40 ns for an input overdrive of 2 mV while consuming 22 µA current. The co-design of comparator and the respective switch can optimize the quiescent loss of the comparator with the ohmic loss of the switch to reduce the overall losses. The block turns on with low output state as soon as the switching node rises a diode above the battery voltage before the switch turns on and turns off as soon as the switch turns off. The digital switches M_4, M_{12}, M_{13}, M_{13}, M_{14}, M_{15}, M_{17}, M_{18}, M_{20}, M_{26} and M_{27} can disable the current paths to power gate the block in CP_O's off state.

5.2.2.8 Battery-Diode Comparator

The battery-diode comparator CP_B in Fig. 5.18 measures voltage across the battery charging switches $M_{B(CHG)}$ and M_B respectively and turns off the switches when the voltage dips below zero. The two stage current mode amplifier in Fig. 5.27 in open loop implements the CP_B comparator. The transconductance gm_I of M_7 and M_{14}, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{SW} and v_{BAT} into a current. M_{10}–M_{18}, M_{11}–M_{23} and M_{15}–M_{20} mirror the current and, the output impedance of M_{20} and M_{23} translate the current to the single ended output that drives the gates of the inverter M_{26}–M_{27}.

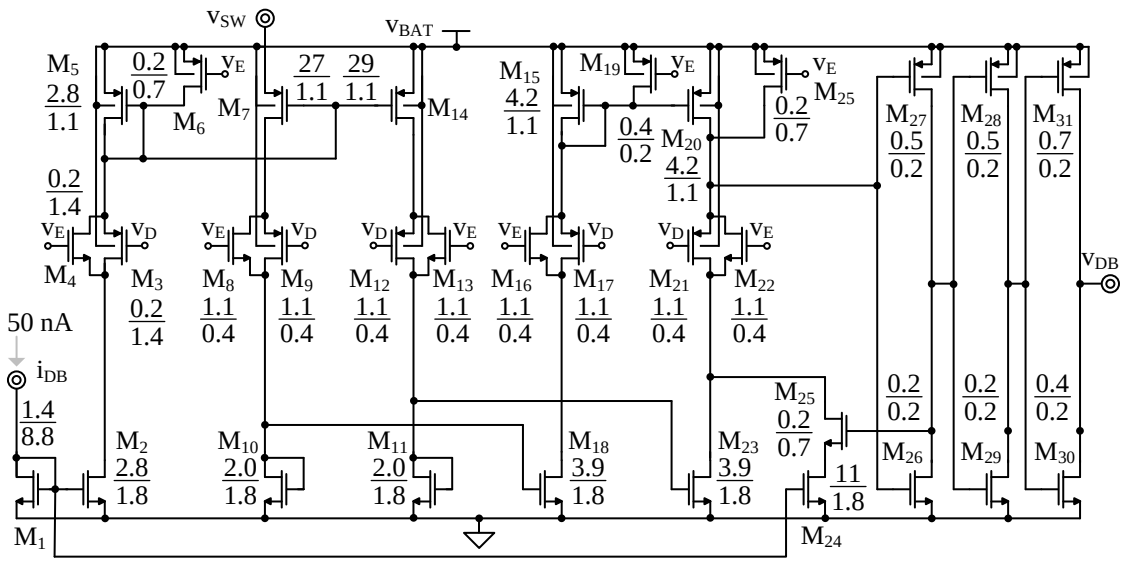


Fig. 5.27. Reversing battery-diode comparator.

The inverters M_{28}–M_{29} and M_{30}–M_{31} buffer the signal to the output v_{DB}. With the output of the inverter M_{26}–M_{27} high, M_{25} engages M_{24} to pull M_{26}–M_{27}'s gate low and reinforce the high state at its output. This way M_{24} sets a 5 mV hysteresis so that v_{DB} doesn't shuttle back and forth as the switch turns off. The difference in size between M_7 and M_{14} introduces a slight offset to aid the comparator switch state exactly at the zero crossing point of the switch voltage, in Fig. 5.18. In the absence of the offset Fig. 5.1 the comparator will detect zero crossing only after sufficient overdrive builds in the opposite direction, or in other words the switch current builds up sufficiently in the negative direction and thereby leading to larger losses. M_1–M_2 mirrors and scales the 50-nA bias current from the bias block to set the bias voltage at the gate of M_5 and gm_I of the input differential stage.

The comparator has a delay of less than 30 ns for an input overdrive of 2 mV while consuming 33 µA current. The co-design of comparator and the respective switch can optimize the quiescent loss of the comparator with the ohmic loss of the switch to

reduce the overall losses. The block turns on with low output state as soon as the switching node raises a diode above the battery voltage before the switch turns on and turns off as soon as the switch turns off. The digital switches M_3, M_4, M_6, M_8, M_9, M_{12}, M_{13}, M_{16}, M_{17}, M_{19}, M_{21}, M_{22} and M_{25} can disable the current paths to power gate the block in CP_B's off state.

5.2.2.9 Ground-Diode Comparator

The ground-diode comparator CP_G in Fig. 5.18 measures voltage across the ground switch M_G respectively and turns off the switches when the voltage dips below zero. The two stage current mode amplifier in Fig 5.28 in open loop implements the CP_G comparator. The transconductance gm_I of M_7 and M_8, that operate near subthreshold to maximize g_M amplifies, the voltage difference between v_{SW} and ground into a current. M_{32}–M_{14}, M_{13}–M_{22} and M_{17}–M_{19} mirror the current and, the output impedance of M_{19} and M_{22} translate the current to the single ended output that drives the gates of the inverter M_{26}–M_{27}. The inverters M_{28}–M_{30} and M_{29}–M_{30} buffer the signal to the output v_{DG}.

With the output of the inverter M_{26}–M_{27} high, M_{24} engages M_{25} to pull M_{26}–M_{27}'s gate low and reinforce the high state at its output. This way M_{25} sets a 5 mV hysteresis so that v_{DG} doesn't shuttle back and forth as the switch turns off. The difference in size between M_7 and M_8 introduces a slight offset to aid the comparator switch state exactly at the zero crossing point of the switch voltage, in Fig. 5.18. M_1–M_2 mirrors and scales the 50-nA bias current from the bias block to set the bias voltage at the gate of M_5 and gm_I of the input differential stage.

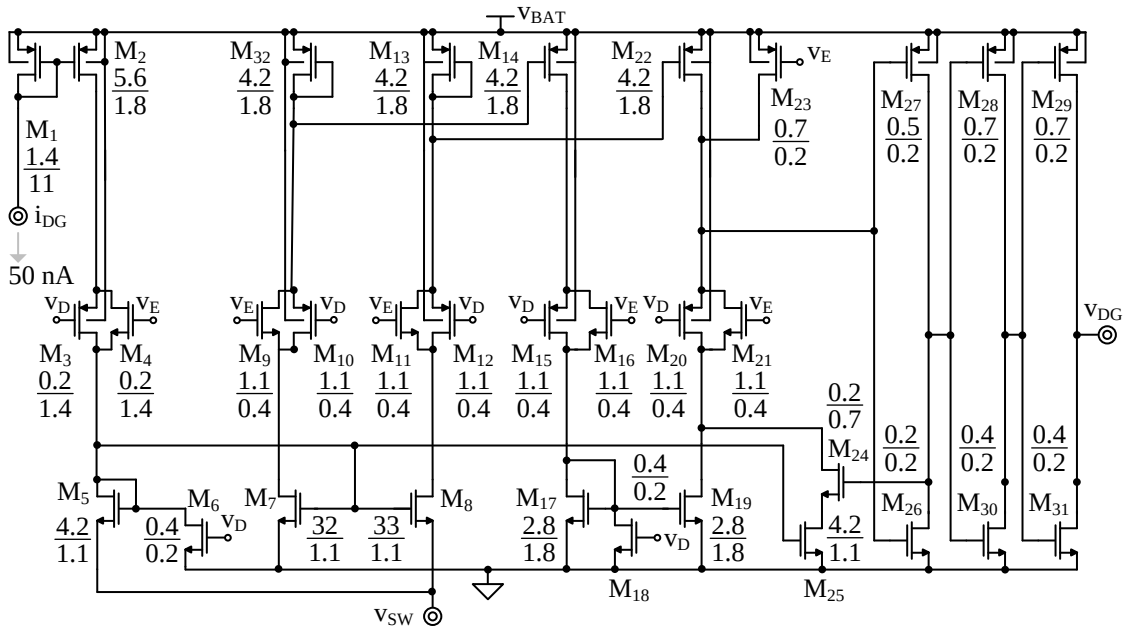


Fig. 5.28. Reversing ground-diode comparator.

The comparator has a delay of less than 30 ns for an input overdrive of 2 mV while consuming 42 µA current. The co-design of comparator and the respective switch can optimize the quiescent loss of the comparator with the ohmic loss of the switch to reduce the overall losses. The block turns on with low output state as soon as the switching node drops a diode below the ground voltage before the switch turns on and turns off as soon as the switch turns off. The digital switches M_3, M_4, M_6, M_9, M_{10}, M_{11}, M_{12}, M_{15}, M_{16}, M_{18}, M_{20}, M_{21} and M_{23} can disable the current paths to power gate the block in CP_G's off state.

5.2.2.10 Fixed On-Time Delay

Fig. 5.29 presents the circuit that implements the 700-µs battery packet energizing time in Fig. 5.18. In Fig. 5.14 the M_5–M_6 charges capacitor C_{DLY} till its voltage cross trip point where M_{10}'s current exceeds M_{14}'s via switch M_{15}. After this trip point M_{11}'s source

drops and increases M_{11}'s current to raise it above M_{13}'s and pulls the gate of M_{15}, M_{17} and M_{18} low. The inverters M_{19}–M_{20} and M_{21}–M_{22} buffer the signal, and set the output latch to set the output v_{DLO} high.

The circuit engages at the rising edge of the input v_{DLI} through the inverters M_1–M_2 and M_3–M_4, the rising edge detector and the input SR latch. This way in Fig. 5.29 the output v_{DLO} turns high 700 µs after v_{DLI} turns high and turns low immediately as v_{DLI} turns low through the resetting of the output SR latch. The digital switches M_7, M_8, M_{12} and M_{16} turns off and power gates the delay block when not in use.

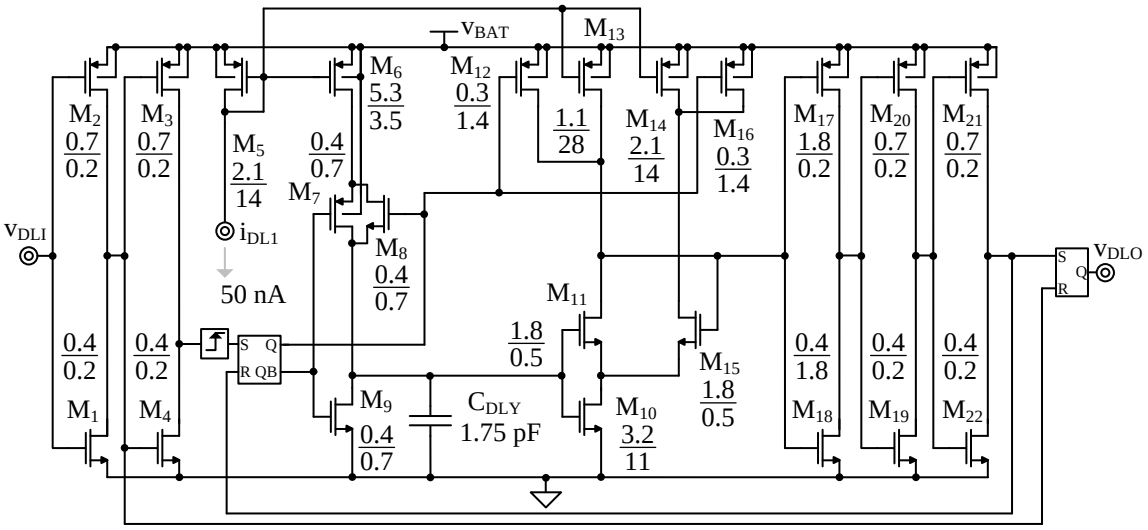


Fig. 5.29. Reversing fixed on-time delay.

5.2.2.11 PTAT Bias Current Generator

The proportional to absolute temperature (PTAT) bias current generator in Fig. 5.30 generates and supplies the bias currents for all the comparators and amplifiers in the system. For this, M_4 and the 8 times bigger M_5 apply the difference in gate source voltage around 60 mV across an external 1.2 MΩ resistor to generate a 50 nA current. As the

transistors operate in subthreshold, the difference in the gate source voltages has a proportional to temperature coefficient. The PTAT current increases with temperature and ensure the bias currents that run the comparator scale and dominate as transistor leakage currents increase with temperature.

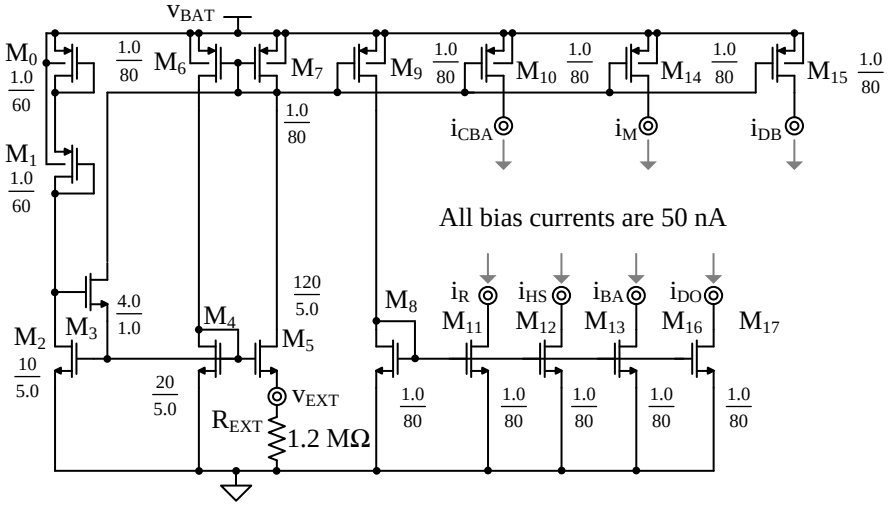


Fig. 5.30. Reversing PTAT bias current generator.

The transistor M_4, M_5, M_6, M_7, M_8 and M_9 form a positive feedback loop that latches the current at a stable operating point of 50 nA. However, zero current condition is also a stable operating point, and M_1, M_2 and M_3 form a startup circuit to pull the circuit out of zero current state. When M_4 and M_5 conduct zero current M_2 is off and M_1 pulls the gate of M_3 high, M_3 turns on to leak current from the gate of M_9 and M_8 to push the latch away from zero current. At the desirable operating point M_2 conducts enough current to turn off M_3. The transistors M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}, M_{21} and M_{22} mirrors the 50 nA bias current bias the different blocks. Overall the always on bias block consumes about 800 nA through its various legs. Reducing the magnitude of the single leg current below 50 nA can reduce the quiescent losses and

improve the low power efficiency of the system, however this can make the circuits sensitive to the substrate noise.

5.2.3 Power Switches

In the reversing switching circuit of Fig. 5.18 M_{PV}, M_G and $M_{O(SUP)1}$–$M_{O(SUP)2}$ and M_B transfers 10–130 µW photovoltaic power to the output and M_B, M_G and $M_{O(AID)}$ transfers up to 10 mW battery power to the output. The circuit scales the frequency of PV packets with P_{PV} and number of fixed-size battery packets with P_{LD}.

5.2.3.1 Ground Switch

Design: The ground switch M_G in Fig. 5.18 and Fig. 5.31 has two parts, only fraction of the switch engages during lower power heavily sourced mode and the entire switch engages during higher power battery assisted mode. In the heavily sourced mode the smaller area ground switch engages during the energizing time of the PV packet. In this mode during the on time of the switch, the switch current rises from zero to the PV packet peak current of 11 mA. In the battery-assisted mode the entire switch engages during the energizing time of the PV packet as in heavily sourced mode and also during the de-energizing time of each battery packet. In this mode during the de-energizing time of the battery packet as the switch engages the switch current quickly rise to the inductor peak current of 31 mA and falls to zero during the on-time of the switch.

The switch that implements M_G is a NMOS switch in Fig. 5.31 as the NMOS conducts low voltages more efficiently and the body diode of the switch provides dead time current path for the inductor current that flows away from the v_{SWB} node in Fig.

5.18. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the smaller switch at 1050 µm, in Fig. 5.31, that presents a series resistance of 0.6 Ω balances both the ohmic, gate-drive loss for the PV packet. In battery-assist mode the entire 3000 µm switch engages during the battery packet de-energizing time presenting a series resistance of 0.2 Ω. As only the frequency of the constant size PV and battery packet varies with P_{PV} and P_{BAT}, both the ohmic losses and switching losses scale with P_{PV} and P_{BAT} as switch size only depends on the type of packet. This way the two different switch sizes for the two modes is optimum across P_{PV} and P_{BAT}. The ground diode comparator CP_G that measure voltage across switch has a inbuilt trimmable offset that allows for decoupling the switch sizing from comparator design.

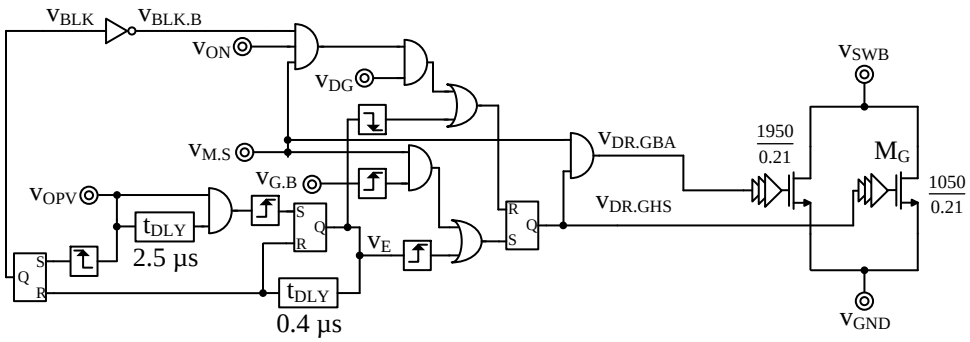


Fig. 5.31. Reversing ground switch and driving logic.

Switching Logic: The signals that determine the gate drive signals $v_{DR.GHS}$ and $v_{DR.GBA}$ are the gate signal $v_{G.B}$ of M_B, the output of ground diode comparator v_{DG}, output of the photovoltaic comparator v_{OPV}, the output of the battery-assist comparator v_{ON} and $v_{M.S}$. The digital circuit in Fig. 5.31 implements the driving logic for M_G switch. In Fig. 5.31 the rising edge of v_{OPV} sets the bottom left SR latch that drives the blank time signal v_{BLK}.

v_{BLK} ensures a blank time of 2.5 µs after CP_{PV} triggers when no battery packet transfer occurs. The SR latch is rest after the energizing time of the PV packet. In heavily sourced mode the v_{OPV} after the blank time delay sets the SR latch that drive the PV packet energize signal v_E high. This SR latch resets after the 400ns, this way defining the size of the PV packet. A OR gate propagates v_E and its rising edge sets the SR latch that drives $v_{DR.GHS}$. The falling edge of v_E resets the latch and turns of M_G switch in HS mode.

In battery-assist mode the SR latch that drives $v_{DR.GHS}$ is set every time the battery packet energizing time ends and $v_{G.B}$ goes high to turns M_B off. In this mode the v_{DG} turns the ground switch off when it detects zero crossing point of the inductor current signaling the end of a battery packet. However the ground switch is not reset after v_{ON} falls down or v_{BLK} high to indicate the last battery packet in that PV period. This way the ground switch remains high for the next PV packet, thereby saving one switching event.

5.2.3.2 Photovoltaic Switch

Design: The photovoltaic switch engages for the entire duration in heavily sourced mode and for the duration of the PV packet transfer in battery-assisted mode. The photovoltaic switch M_{PV} in Fig. 5.18 and Fig. 5.32 has two parts, only fraction of the switch engages during battery-assisted mode and the entire switch engages during heavily sourced mode, as the PV switch only switches only in the battery-assisted mode. During the on time of the switch, the switch current which is same as the inductor PV-packet current rises from zero to 11 mA in 0.4 µs and drops from 11 mA back to zero in 325 ns while supplying output and 140ns while charging battery, Fig. 4.2 and Fig. 4.4.

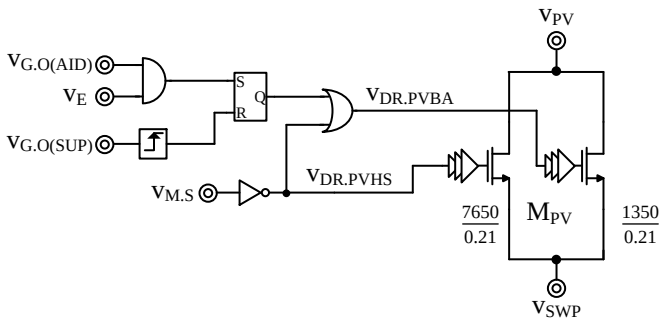


Fig. 5.32. Reversing photovoltaic switch and driving logic.

The switch is NMOS as the NMOS conducts low voltages more efficiently and the photovoltaic voltage is only around 0.3 V. The body diode of the switch provides dead time current path for the inductor current flows out of the v_{SWP} node in Fig. 5.18. The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch 1350 µm, in Fig. 5.32, balances both the ohmic and switching losses and presents a series resistance of 0.66 Ω in the battery-assist mode. As only the frequency of the constant size PV packet varies with photovoltaic power P_{PV}, both the ohmic losses and switching losses scale with P_{PV} and as a result a single switch size is optimum across P_{PV} in battery-assist mode. In heavily sourced mode the PV switch is on all the time and doesn't switch and as a result the switch width can be large at 9000 µm presenting just 0.1 Ω resistance, reducing resistance below 0.1 Ω has little effect on the overall efficiency.

Switching Logic: The digital circuit in Fig. 5.32 implements the driving logic for M_{PV} switch. The signals that determine the driving signals $v_{DR.PVBA}$ and $v_{DR.PVHS}$ for M_{PV} are the gate signals $v_{G.O(AID)}$ of the battery-assist output switch $M_{O(AID)}$ and $v_{G.O(SUP)}$ of photovoltaic output switch $M_{O(SUP)1}$–$M_{O(SUP)2}$, $v_{M.S}$ and v_E. In heavily sourced mode $v_{M.S}$

turns low and driving $v_{DR.PVBA}$ and $v_{DR.PVHS}$ high via inverter and OR gate for the entire during of the heavily sourced mode. In battery-assisted mode a SR latch drives $v_{DR.PVBA}$, the SR latch turns high as soon as the v_E turns high and turns off as PV packet finishes and $v_{G.O(SUP)}$ goes high to turn off $M_{O(SUP)1}$–$M_{O(SUP)2}$.

5.2.3.3 Photovoltaic Output Switch

Design: The photovoltaic output switch $M_{O(SUP)1}$–$M_{O(SUP)2}$, in Fig. 5.18 and Fig. 5.33 engages for the de-energizing time of the PV packet that supplies the load.. During the on time of the switch, the switch current quickly rises to the inductor peak current of 11 mA as it turns on and flows it till the current drops to zero thereby tripping CP_O and turning off the switch. Typically on time of the switch in this mode is 325 ns. The switch that implements the output switch is a back-back PMOS as the PMOS conducts high voltages more efficiently and the back-back body diodes block current flow when the circuit charges battery and as a result the switching node rises to v_{BAT}.

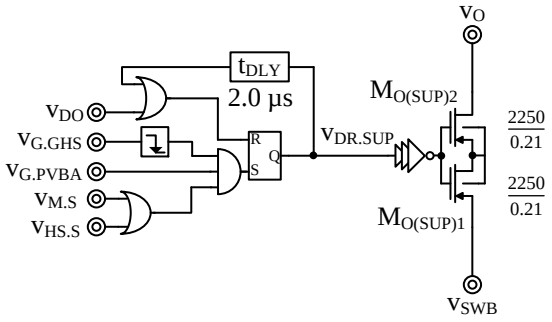


Fig. 5.33. Reversing photovoltaic output switch and driving logic.

The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of each switch at 2250 µm, in Fig. 5.33, balances both the ohmic and gate-

drive loss of the switch. The switch presents a series resistance of around 5 Ω. Adding input offset to the CP_O allows for decoupling comparator overdrive design from the switch width and as a result the resistance of the switch is lower than the non-reversing case despite transferring only the lower energy PV packets. This way adding an offset to the comparator can allow the switch to scale larger and better efficiency. As only the frequency of the constant size PV packet varies with photovoltaic power P_{PV}, both the ohmic losses and switching losses scale with P_{PV}.

Switching Logic: The digital circuit in Fig. 5.33 implements the driving logic for $M_{O(SUP)1}$–$M_{O(SUP)2}$ switch. The signals that determine the gate driving signal $v_{DR.SUP}$ of $M_{O(SUP)1}$–$M_{O(SUP)2}$ are the gate signal $v_{G.GHS}$ of heavily sourced mode part of switch M_G, the gate signal $v_{G.PVBA}$ of battery-assisted mode part of M_{PV}, v_{DO}, $v_{M.S}$, and $v_{H.S}$. In Fig. 5.23 the falling edge of the $v_{G.GHS}$ sets the SR latch that drive $v_{DR.SUP}$ only when $v_{HS.S}$ is high in heavily sourced mode or when system is in battery-assisted mode. $v_{G.PVBA}$ needs to be high for the SR latch to be set, this ensures the $M_{O(SUP)1}$–$M_{O(SUP)2}$ switch turns on only during the PV packet transfer.

The output diode comparator output v_{DO} resets the latch when the PV packet finishes and switch current goes to zero. During the charging up of output voltage v_O from a completely discharged state the PMOS switch cannot pull the switching node v_{SWB} below a threshold voltage above ground. This results in CP_O not tripping even though the inductor current drops to zero and the system control may stall. To prevent this the 2-µs delay block ensures the switch turns remains on for a maximum of 2 µs.

5.2.3.4 Battery Switch

Design: The battery switch M_B in Fig. 5.18 and Fig. 5.34 has two parts, only fraction of the switch engages during lower power heavily sourced mode and the entire switch engages during higher power battery assisted mode. In the heavily sourced mode the smaller area battery switch engages during the de-energizing time of the PV packet that charges the battery. In this mode as the switch turns on the switch current quickly rises to the inductor peak current.

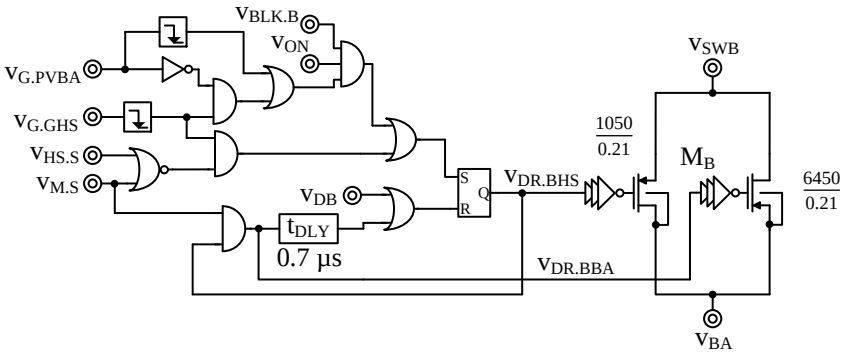


Fig. 5.34. Reversing battery switch and driving logic.

During the on-time of the switch the switch current falls from PV packet peak current of 11 mA to zero. In the battery-assisted mode the entire switch engages during the energizing time of each of the battery packets. In this mode during the energizing time of the battery packet, as the switch engages and the switch current rises from zero to the battery packet peak current of 31 mA during the on-time of the switch. The switch that implements M_B is a PMOS switch in Fig. 5.34 as the PMOS conducts high battery

voltage more efficiently. The body diode of the PMOS switch provides dead time current path for the inductor current that flows towards the switching node v_{SWB} in Fig. 5.18.

The length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the smaller switch at 1050 µm, in Fig. 5.34, that presents a series resistance of 2.4 Ω balances both the ohmic, gate-drive loss for the PV packet. In battery-assist mode the entire 7500 µm switch engages during the battery packet energizing time presenting a series resistance of 0.36 Ω. As only the frequency of the constant size PV and battery packet varies with P_{PV} and P_{BAT}, both the ohmic losses and switching losses scale with P_{PV} and P_{BAT} as switch size only depends on the type of packet. This way the two different switch sizes for the two modes is optimum across P_{PV} and P_{BAT}. The battery diode comparator CP_B that measure voltage across switch during the battery charging phase has an inbuilt trimmable offset that allows for decoupling the switch sizing from comparator design.

Switching Logic: The digital circuit in Fig. 5.34 implements the driving logic of M_B switch. The signals that determine the gate drive signals $v_{DR.BHS}$ and $v_{DR.BBA}$ are the gate signal $v_{G.GHS}$ of M_G, the gate signal $v_{G.P.BA}$ of M_{PV}, the inverted blank time signal $v_{BLNK.B}$, v_{ON}, v_{DB}, $v_{HS.S}$ and $v_{M.S}$. In Fig 5.34 during the heavily sourced mode with $v_{HS.S}$ and $v_{M.S}$ low the falling edge of the $v_{G.GHS}$ sets and v_{DB} resets the the SR latch that drives $v_{DR.BHS}$. In the battery-assisted mode the falling edge of the M_{PV}'s gate signal $v_{G.PVBA}$ at the end of the PV packet or the falling edge of the M_G's gate signal $v_{G.GHS}$ at the end of the battery packet sets the SR latch when v_{ON} and $v_{BLK.B}$ are high. This way the system sends a new battery packet at the end of every PV and battery packet as long the load demands it via

through v_{ON} and the blank time that ensures the non-overalp of the PV and battery packet transfers is not set. The SR latch in this mode is reset after the fixed on-time of 0.7 µs thereby setting the optimum size of the battery packet.

5.2.3.5 Battery-Assist Output Switch

Design: The battery assist output switch $M_{O(AID)}$ switch, in Fig. 5.18 and Fig. 5.35, engages during for the entire duration of transfer of battery packets in the battery-assist mode. In this mode during the on time of the switch, the switch current rises from zero to the battery packet peak current of 31 mA in 700 ns during the energizing phase and falls from 31 mA to zero in 560 ns during the de-energizing phase. This process repeats for the duration of of battery packet transfer in the PV period. In circuit of Fig. 5.18 the number of fixed-size battery packets depends on the load requirement. For instance the for a load power of 10 mW the number battery packets limit cycles between 6 and 7 packets. The battery assist comparator CP_{BA} compares v_{EA} and v_R to set the battery packet energizing time on-time v_{ON} that set the on-time of the switch.

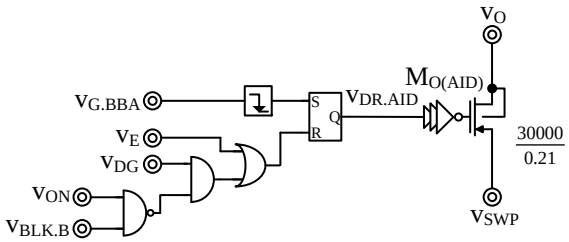


Fig. 5.35. Reversing battery-assist output switch and driving logic.

The switch that implements $M_{O(AID)}$ is a PMOS switch in Fig. 5.35 as the PMOS conducts high voltages more efficiently and the body diode of the switch provides dead time current path for the inductor current that flows into the v_{SWP} node in Fig. 5.18. The

length of the switch is the minimum channel length possible in the technology, 0.18 µm, as it contributes proportionally to both ohmic and gate-drive losses. The width of the switch at 30000 µm, in Fig. 5.35, balances both the ohmic, gate-drive loss for the mid-range load power of 5 mW. The switch presents a series resistance of around 0.2 Ω. At higher power levels the switch is less optimum and the ohmic losses dominate over gate-drive losses, but with an inductor ESR of 2 Ω, the ohmic losses are insignificant. In the lower power levels for instance the battery packets limit cycle between 1 or 2 the gate-drive losses dominate the losses of the switch and efficiency drops. In the circuit Fig. 5.18 loss associated with $M_{O(AID)}$ is the only one that does scale proportionally with P_{LD}.

Switching Logic: The digital circuit in Fig. 5.35 implements the driving logic of $M_{O(AID)}$ switch. The signals that determine the gate driving signal $v_{DR.AID}$ of $M_{O(AID)}$ are the gate signal $v_{G.BBA}$ of M_B, v_E, v_{DG}, v_{ON} and $v_{BLK.B}$.. In Fig 5.35 the falling edge of the $v_{G.BBA}$ sets the SR latch that drive $v_{DR.AID}$ only in the battery assist mode. The latch is reset at by v_{DG} going high during the low state of v_{ON} or $v_{BLK.B}$ indicating the last battery packet. The high state of v_E resets the battery-assist output switch to prevent shorting of the battery and PV cells in case of faults.

5.3 Summary

This chapter presents the design implementation of the two different power stages reversing and non-reversing and the control blocks that implement the feedback control, variable packet control for non-reversing case and multiple packet control for the reversing case. In the non-reversing switching circuit of Fig. 5.1 M_{PV}, M_{G2} and M_{O1}–M_{O2} and $M_{B(CHG)}$ transfers 10–100 µW photovoltaic power to the output and $M_{B(AID)}$, M_{G1} and

M_{O1}–M_{O2} transfers up to 1 mW battery power to the output. The circuit scales the frequency of PV packets with P_{PV} and size of the battery packet with P_{LD}. In the reversing switching circuit of Fig. 5.18 M_{PV}, M_G and $M_{O(SUP)1}$–$M_{O(SUP)2}$ and M_B transfers 10–130 µW photovoltaic power to the output and M_B, M_G and $M_{O(AID)}$ transfers up to 10 mW battery power to the output. The circuit scales the frequency of PV packets with P_{PV} and number of fixed-size battery packets with P_{LD}.

In both implementations the co-design of switches and controller and, duty cycling of control blocks improves efficiency. The reversing implementation improves upon the non-reversing implementation by using variable number of packets instead of variable size one and this way improves efficiency by scaling most of the losses proportional to load power. The reversing implementation also introduces variable switching to optimize switch sizes for the lower energy PV packet and higher energy battery packet transfer, as well as offsets in diode comparators to decouple the comparator design from switch design. Overall the sizing of switches, the sequence in which they engage and duty-cycling of control blocks on the basis of the functions they implement are important considerations for high efficiency low power design.

CHAPTER 6. PHOTOVOLTAIC CHARGER–SUPPLY SYSTEM

The battery-assisted single photovoltaic cell harvesting charger–supply system in this work consists of the photovoltaic cell that acts as the energy source, the battery that acts as the power source and energy buffer, the power flow management integrated circuit that manages the efficient transfer of power between the PV cell, battery and the load. The switched inductor power stage consists of an external inductor L_X for efficient power transfer, input capacitor C_{IN} and output capacitor C_{OUT} that restricts the ripple across the PV cell v_{PV} and the load v_O respectively. This work relies on a manual control adjustment of the photovoltaic period in one prototype and regulation of the photovoltaic voltage in the second prototype for tracking the PV cells maximum power point. Therefore the Section 6.1 considers the photovoltaic loop and how the two options fit into a regulation loop. Section 6.2 and Section 6.3 discusses the full system implementation for the reversing and non-reversing prototypes and test circuits. Finally Section 6.4 presents the system performance in light of other state of the art implementation. Sections 6.5 highlight the contributions of this research and Section 6.6 discusses future work.

6.1 Photovoltaic Regulation

As Chapter 2 shows the photovoltaic cell generates maximum power at a particular voltage for each light intensity level. Therefore the power flow management IC should have the capability to continuously extract maximum power at a particular lighting condition and should also be able to change its operating point with change in intensity of light.

6.1.1 Photovoltaic Loop

The photovoltaic regulation loop consists of the PV cell, the charger–supply IC and the maximum power tracking circuits. The primary function PV regulation loop is to extract maximum available power from the PV cell and supply the load or recharge the battery with it. Fig. 6.1 shows the block level signal processing in a PV regulation loop. In this loop the maximum power point circuit block provides a control signal C, for example v_{MPP} or f_{MPP}, that biases the charger–supply system at a particular operating point and samples a measure of the photovoltaic power or output power P_{PV}' to continuously regulate the system. Sampling the output power P_{PV}' has the advantage of including the charger–supplies losses in the power optimization loop. Here the relationship between the control signal and P_{PV}' is generally hill shaped with maximum P_{PV}' corresponding to only one particular value of the control variable.

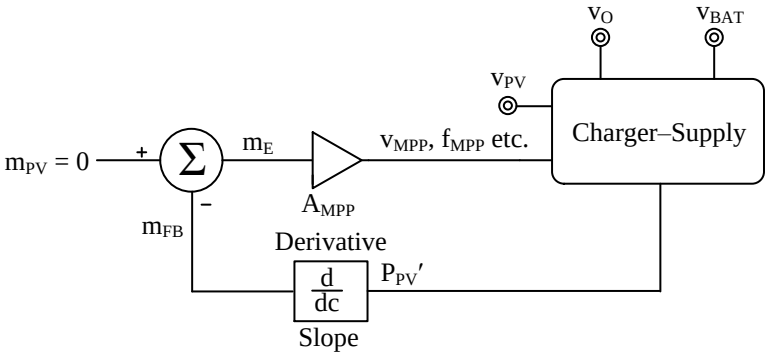


Fig. 6.1. Photovoltaic regulation loop.

The maximum power tracking circuits include the slope block, the summing stage, the target reference and the translating amplifier A_{MPP}. The slope block generates the gradient m_{FB} of change of P_{PV}' with C. As the Chapter 3 shows, for a hill profile, at the maximum power point the gradient of P_{PV}' is zero. As a result in this loop the target

reference m_{PV} for the slope of P_{PV}' with respect to control signal C is zero. The summing block further generates the error m_E in the slope with respect to zero. In other words m_E is difference between m_{PV} and m_{FB}. The maximum power point amplifier A_{MPP} amplifies and translates m_E to the maximum power point control signal C.

This dissertation work doesn't include the maximum power point loop but uses the maximum power point control signal and manually adjusts it according to the light level. In case of the non-reversing prototype an external clock whose frequency varies with light level is the control signal that drives the charger–supply circuit. The charger–supply circuit extracts a fixed energizing time energy packet from the photovoltaic cell at very rising edge of the clock, Fig. 6.2.

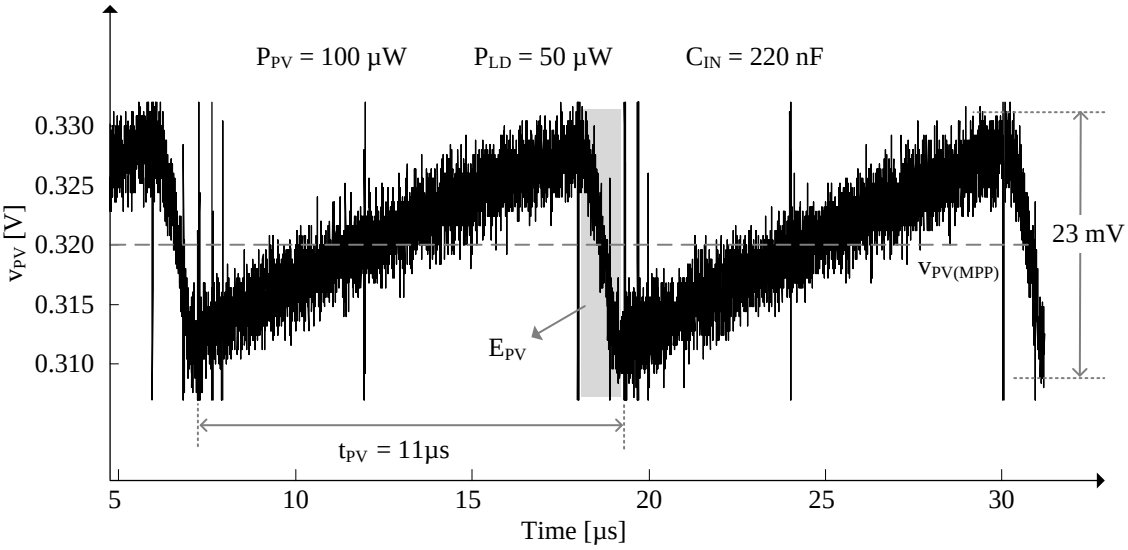


Fig. 6.2. Measured non-reversing photovoltaic voltage.

In Fig. 6.2 the time period of the PV clock is around 11 µs for a P_{PV} of 100 µW and the v_{PV} ripples around the maximum power point value of 0.32 V with a peak-to-peak ripple of 23 mV. At a frequency higher than this value the photovoltaic voltage will

be lower than the maximum power point and vice-versa for lower photovoltaic frequency. This way as P_{PV} varies between 10–100 µW the PV clock frequency varies between 8–85 kHz.

In case of the reversing circuit the control signal is the photovoltaic peak voltage reference v_{MPP}, Fig 6.3. The photovoltaic comparator CP_{PV} in Fig. 5.18 and Section 5.2.2 compares v_{PV} with v_{MPP} and extracts a PV energy packet every time v_{PV} crosses v_{MPP}. As a result v_{PV} falls after v_{PV} exceeds v_{MPP}. Light energy then charges the PV cell to recover v_{PV} voltage back to v_{MPP} and the process repeats. It is interesting to note that the maximum power control signal v_{MPP} is offset from the $v_{PV(MPP)}$ and the maximum power point loop accounts for this difference via feedback while setting v_{MPP}.

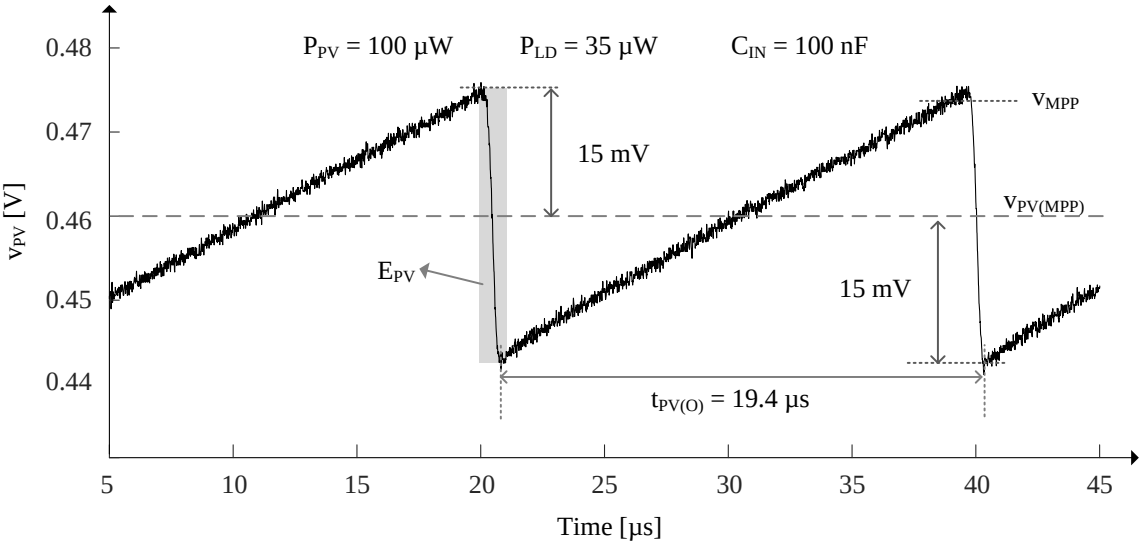


Fig. 6.3. Measured reversing photovoltaic voltage.

In Fig. 6.3 v_{MPP} is around 0.475 for a P_{PV} of 130 µW and the v_{PV} ripples around the maximum power point value of 0.46 V with a peak-to-peak ripple of 30 mV. As the

photovoltaic power increases v_{MPP} increases with it and this way as P_{PV} varies between 10–130 µW, v_{MPP} varies between 0.4–0.5 V.

6.1.2 Photovoltaic Capacitance

The photovoltaic loop sets the operating point of the charger–supply about maximum power point. The purpose of C_{IN} in Fig. 5.1 and 5.18 is to reduce this ripple, to keep v_{PV} near its optimal setting, near its maximum power point. For this, C_{IN} captures and supplies what L_X and v_{PV} do not. In fact, since L_X conducts for a small fraction of t_{PV} to sustain P_{PV}, Section 4.1.1, i_L is much higher than i_{PV} across this time and C_{IN} supplies most of i_L's charge q_L. So to limit the input ripple to Δv_{PV}, C_{IN} should be roughly

$$C_{IN} = \frac{\Delta q_C}{\Delta v_{PV}} \approx \frac{\Delta q_L}{\Delta v_{PV}} = \frac{0.5 v_{LE}\, t_{PE}{}^2 + 0.5 v_{LD}\, t_{PD}{}^2}{\Delta v_{PV} L_X}, \tag{6.1}$$

where v_{LE} and v_{LD} are L_X's energizing and de-energizing voltages v_{PV} and $v_O - v_{PV}$.

In the non-reversing circuit of Fig. 5.1 to keep the PV cell at its maximum power point $P_{PV(MPP)}$, v_{PV} should be steady at 0.32 V, which only happens when output current of PV cell i_{PV} is 312 µA. But since L_X does not connect continuously to v_{PV}, i_{PV} is not steady. The input capacitor C_{IN} can absorb and output the difference; but still, C_{IN} cannot keep v_{PV} from altogether changing. This means, the cell, on average, outputs less power than $P_{PV(MPP)}$. With 10 nF, for example, v_{PV} in Figs. 6.4 and 6.5 ripples between 0.13 and 0.39 V. v_{PV} dips to 0.13 V when the system draws an energy packet from v_{PV}, and since D_{PV} leaks exponentially less current at lower voltages, C_{IN} charges more quickly when v_{PV} is lower. v_{PV} is therefore more often near its peak than its valley, and v_{PV} averages to 0.3 V and PV power to 83 µW, which is less than $P_{PV(MPP)}$'s 100 µW.

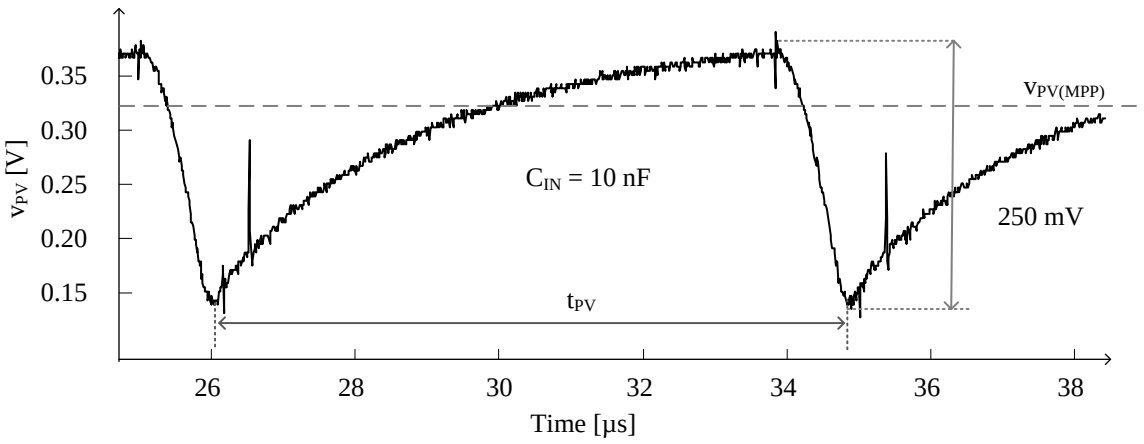


Fig. 6.4. Measured photovoltaic voltage for 10 nF capacitance.

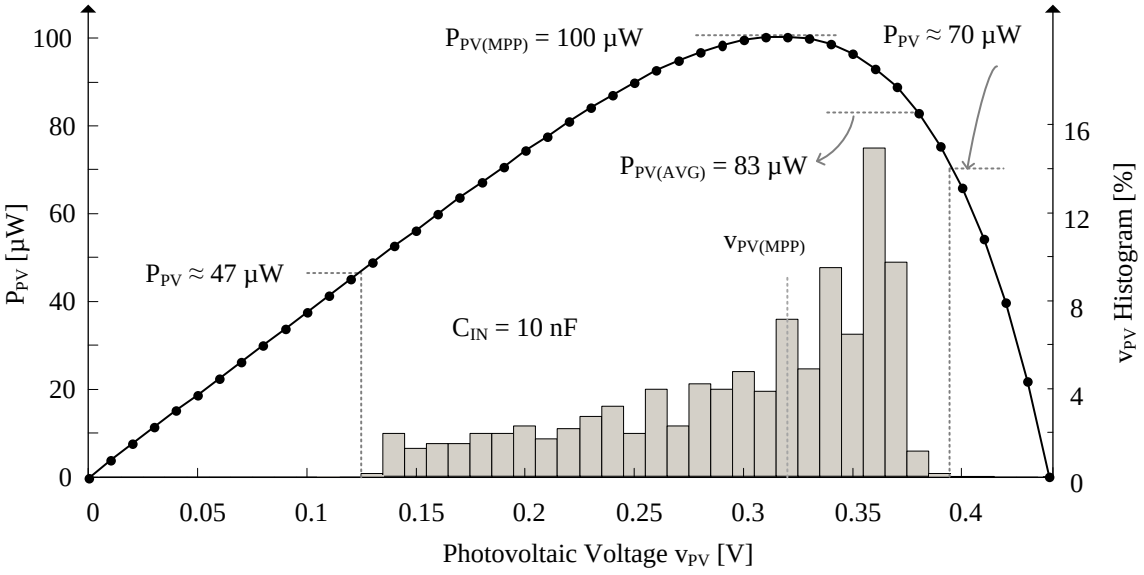


Fig. 6.5. Power profile and voltage histogram of the photovoltaic cell.

Not surprisingly, higher input capacitances suppress v_{PV}'s ripple Δv_{PV} in Fig. 6.6, from 548 mV with the 10 pF that a probe adds to the board to 6 mV when C_{IN} is 1 µF. Above 100 nF, variations in the maximum possible average power are minimal because P_{PV} in Fig. 6.5 is less sensitive to small v_{PV} fluctuations near its maximum power point $P_{PV(MPP)}$. So with 220 nF, which produces ±16 mV ripple, PV power is 99% of $P_{PV(MPP)}$, and marginally higher with higher C_{IN} values. Below 100 nF, P_{PV} is more sensitive. Plus,

the system lengthens t_{PV} when drawing less PV power, so C_{IN}'s ripple grows quickly with lower P_{PV}. As a result, $P_{PV(AVG)}$ drops 60 µW when C_{IN} falls to 1 nF. Interestingly, variations are less severe below 1 nF. This is because the cell's inherent capacitance C_{PV} begins to dominate and saturate the effects of C_{IN}.

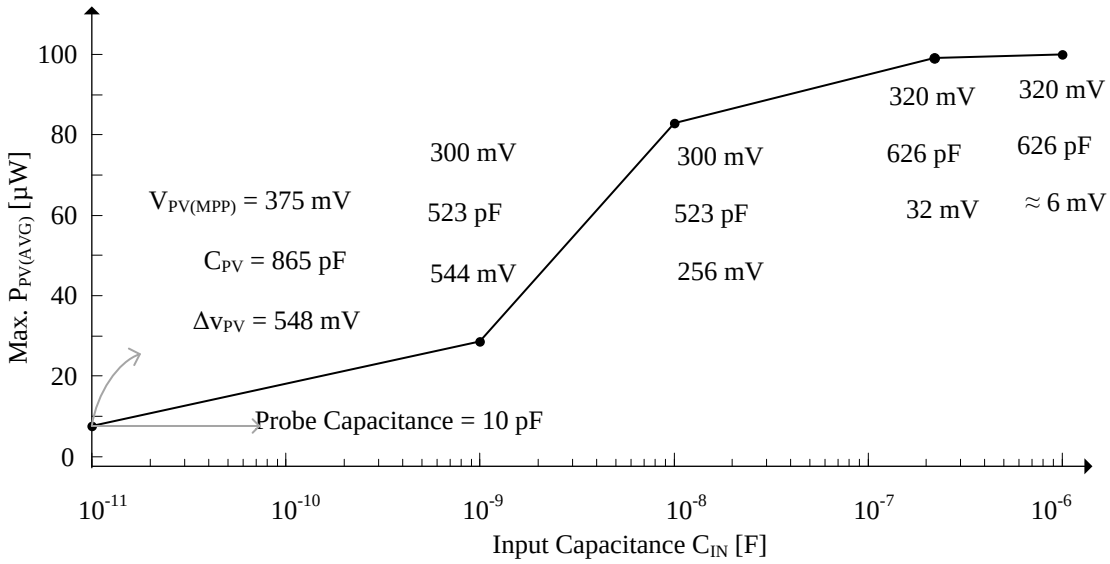


Fig. 6.6. Measured photovoltaic power across input capacitance.

Generally, the PV cell outputs more power when C_{IN} is higher, but since larger C_{IN}'s occupy more board space and P_{PV} is less sensitive to C_{IN} above 100 nF, raising C_{IN} beyond 100–200 nF is difficult to justify. v_{PV}'s maximum power point $V_{PV(MPP)}$ shifts 20 mV from 300 to 320 mV when C_{IN} rises above 1 nF. The drift is more severe below 1 nF because the ripple pulls v_{PV} below ground. So with only 10 pF, $V_{PV(MPP)}$'s variation is not only higher but also in the opposite direction (countering effects of a negative voltage). The photovoltaic capacitance of 220 nF for the non-reversing circuit and 100 nF for the reversing circuit restricts v_{PV} between ±16 mV and ±20 mV.

6.2 Non-Reversing Performance

6.2.1 System

In a wireless microsystem various components stack together vertical and horizontally so as to achieve minimum volume. The wireless micros sensor system includes the PV cell, power flow management IC, battery load, capacitors, inductor and the load all connecting together to with bond wires. The system design include sizing of the capacitors, inductor, PV cell so as to achieve maximum power density while meeting requisite performance such as efficiency and regulation. The photovoltaic input capacitance C_{IN} as Section 6.1.2 shows depends on restricting PV voltage ripple and is a tradeoff between capacitance value and maximum deviation from PV peak power. The output capacitance value depends on restricting the output ripple to less than ± 10% deviation from reference value and thereby reducing supply noise injection into the sensor load. The ESR of the inductor $R_{ESR.L}$ scale inversely with volume and proportionally with the inductance value, inductance value also determines the rate of energizing and de-energizing an inductor. As a result the sizing of inductor is tradeoff between inductor volume, $R_{ESR.L}$ losses and peak transferable power.

The 610 × 610-μm^2 fabricated 0.18-μm CMOS die and the 4 × 4-mm^2 SOIC package that houses it in Fig. 5.2 and Fig. 6.7 house the MOS switches, drivers, comparators, logic, timer circuit, and transconductor in Fig. 5.1. L_X's 47 μH, C_{IN}'s 0.22 μF, and C_O's 2.2 μF are off chip, and L_X occupies 3 × 3 × 1.5 mm^3 and C_{IN} and C_O each occupy 1.6 × 0.8 × 0.9 mm^3. For testability, the 3 × 3 × 1-mm^3 PV cell v_{PV} from Hamamatsu, the compensating 2-nF–1.2-MΩ C_{BA}–R_{BA} filter; and the maximum power-

point tracking clock f_{CLK} are also off chip. This PV cell generates around 100 $\mu W/mm^2$ from incident solar light and, 1 $\mu W/mm^2$ from an indoor light that is 2 m away.

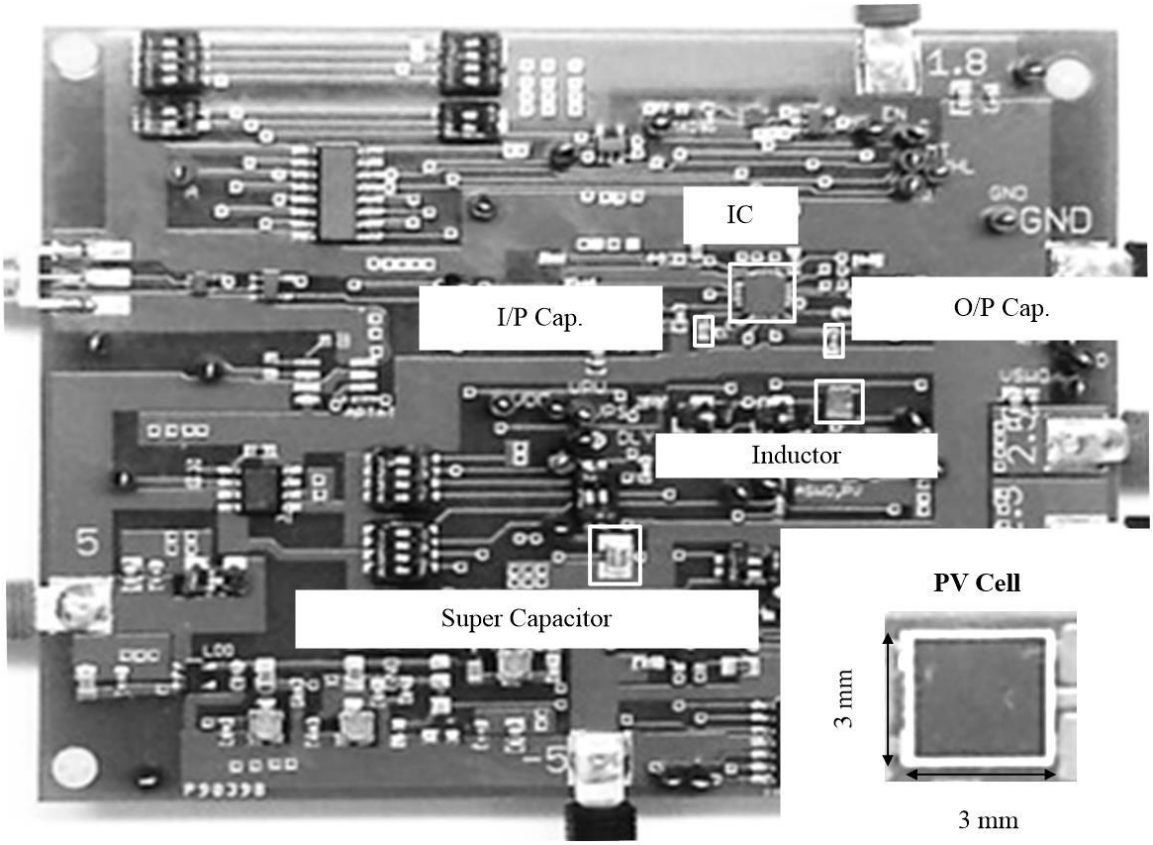


Fig. 6.7. Photographs of the non-reversing circuit board and photovoltaic cell.

6.2.2 Energy Management

Energy management in the different circuit block in the power flow management ICs Fig. 5.1 and Fig. 5.18 are critical for achieving high efficiency at low power levels. Unfortunately, the switches and the controller in Fig. 5.1 and Fig. 5.18 dissipate ohmic, gate-drive, and quiescent power. But as already mentioned in Chapter 3 and Chapter 5, appropriate switch and controller design optimizes the ohmic, gate-drive and quiescent

losses. The rest of the section presents the energy management strategy for the non-reversing prototype.

The major control blocks in the design, in Fig. 5.1, are error amplifier G_{BA}, battery-assist comparator CP_{BA}, heavily source comparator CP_{HS}, mode-detect comparator CP_M and the diode comparators CP_O and CP_B. The power switches in this design are M_{PV}, M_{G2}, M_{G1}, M_{O1}–M_{O2}, $M_{B(CHG)}$ and $M_{B(AID)}$. As already mentioned in Chapter 5, selected switch dimensions balance ohmic and gate-drive losses when the PV cell supplies 100 µW and the load sinks 500 µW, which is half its full range. Under these conditions, when battery-assisted, the switches dissipate 35.2 µW, as Table 6.1 shows. But when only loaded with 40 µW, the switches burn less power at 5.55 µW because the system is no longer drawing assistance from the battery. And with 2 Ω of equivalent series resistance, L_X's $R_{ESR.L}$ burns 7.70 µW when battery-assisted and 5.55 µW when heavily sourced. The switch sizes don't vary depending on the mode and as a result the losses dominate in battery-assisted mode when P_{LD} crosses 500 µW.

Table 6.1. Energy and power loss distribution for non-reversing implementation

Blocks	Energy per Cycle [pJ]	Average Power [µW]
CP_M	7.86	0.68
Heavily Sourced (when P_{PV} = 100 µW and P_{LD} = 40 µW)		
CP_{HS}	25.3	2.20
CP_O	26.9	2.34
CP_{CH}	16.4	1.42
$R_{ESR.L}$	31.3	2.72
Switches	66.8	5.55
Battery-Assisted (when P_{PV} = 100 µW and P_{LD} = 500 µW)		
G_{BA}	80.7	7.02
CP_{BA}	8.43	0.73
CP_O	86.2	7.50
$R_{ESR.L}$	88.5	7.70
Switches	405	35.2

6.2.3 Power-Conversion Efficiency

Power-conversion efficiency η_C refers to what fraction of the power drawn reaches the output. The PV cell is always a source of energy, the load always consumes energy and battery can either store or supply energy. Since the PV cell both supplies the load and charges the battery when heavily sourced, battery power P_{BAT} in this mode is part of output power P_O and η_C is therefore the fraction of P_{PV} that reaches the battery as P_{BAT} and the load as P_{LD}:

$$\eta_C\big|_{HS} \equiv \frac{P_O}{P_{IN}} = \frac{P_{LD} + P_{BAT}}{P_{PV}} \tag{6.2}$$

When battery-assisted, however, the system derives power from the PV cell and the battery, so P_{BAT} is part of input power P_{IN} and η_C in this mode is the fraction of P_{PV} and P_{BAT} that reaches the load as P_{LD}:

$$\eta_C\big|_{BA} \equiv \frac{P_O}{P_{IN}} = \frac{P_{LD}}{P_{PV} + P_{BAT}} \tag{6.3}$$

Notice that the system first drew from the PV cell (when heavily sourced) the battery energy delivered when battery-assisted. So to deliver battery energy, the system loses power during both the heavily- and lightly-sourced states, which when considered across time, η_C as just defined comprehends. Regardless, ohmic and gate-drive power for the switches and duty-cycled power to the controller keep the system from delivering as much power as it receives, so η_C is never 100%.

Across modes, the η_C defined and graphed in Fig. 6.8 peaks at 86% when load power is 0.5 mW and PV power is 100 µW because switch dimensions balance ohmic and gate-drive power at this setting. η_C falls with heavier loads and lower PV power because quadratic ohmic losses when conducting energy packets outpace linear increases in drawn battery power.

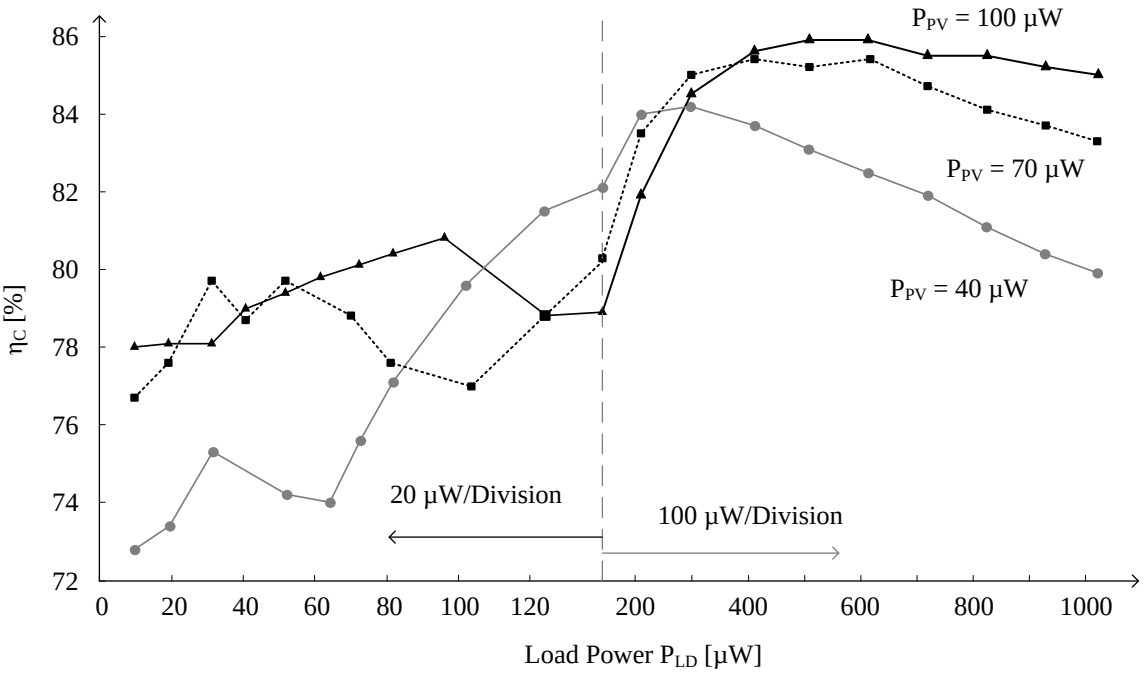


Fig. 6.8. Measured power-conversion efficiency across load and PV power.

η_C also falls with lighter loads because gate-drive and non-duty-cycled controller losses do not scale with output power, so losses become a larger fraction of the power delivered. And since G_{BA} and CP_{BA} in the PWM loop consume more power than CP_{HS} in the hysteretic loop, efficiency is generally lower when lightly sourced than when heavily sourced.

6.3 Reversing Performance

6.3.1 System

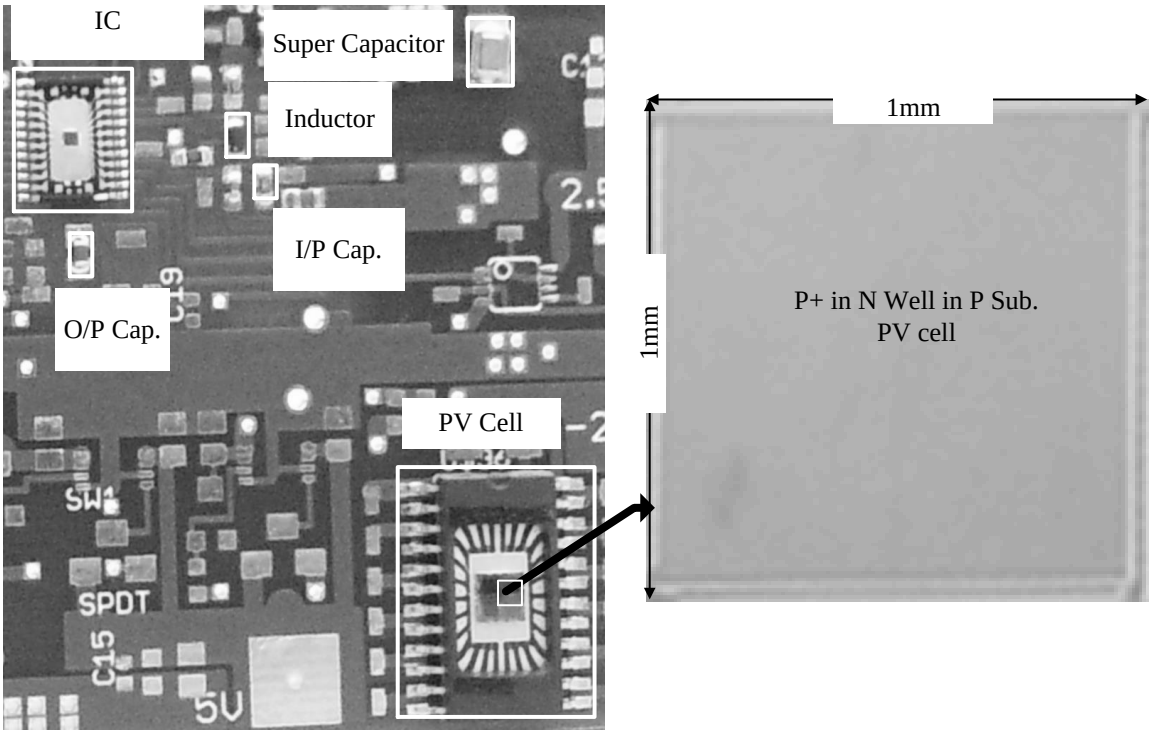


Fig. 6.9. Photographs of the reversing circuit board and photovoltaic cell.

The charger–supply system in Fig. 6.9, transfers power from a 0.35-µm CMOS size PV cell, with a single external inductor, and using the switching converter IC built in 0.18-µm CMOS technology. The 1 × 1-mm^2 P^+ in N well in substrate CMOS PV cell generates 130 µW from the equivalent of solar light. The 900 × 900-mm^2 CMOS die incorporates the power switches, the circuits CP_M, CP_{PV}, CP_{HS}, G_{BA}, CP_{BA}, the ramp generating circuits, fixed-size delays, 2-MΩ R_{BA} and 50 pF C_{BA} filter and the test circuits in Fig 5.18 and Fig. 5.4. The system further use a 1.0 × 0.5 × 0.5-mm^3 100-nF input capacitor C_{IN} and 1.6 × 0.8 × 0.8-mm^3 10-µF output capacitor C_O. This work allows the

use of either a 18-µH inductance, 1-Ω ESR, inductor that occupies 3 × 3 × 1.5 mm^3 for higher efficiency or 22-µH inductance, 2-Ω ESR, inductor that occupies 1.6 × 0.8 × 0.8 mm^3 for smaller footprint.

Integrated Test Circuits: The test circuits, in Fig. 5.2 and Fig 5.18, help debugging faults in the design and in characterization of each block, evaluation of the circuit performance and adjusting circuit performance. There are several methods to evaluate circuits the most direct method is to measure the node voltage and path currents in circuit at different phases of operation. Routing the signal to pins in the IC is one such way of measuring voltage and currents. However perimeter of the die and space each bond pad requires for connection to a pin restricts the number of test pins, which is in addition to the functional pin that the system requires to normal functioning. The test multiplexer and de-multiplexer in Fig. 6.10 helps in reusing a single pin to extract multiple outputs and drive different inputs. T_1, T_2, T_3, T_4, T_5 and T_6 are test pins that select one among output signals v_{DB} to $v_{G.PVBA}$ reach the output pin $v_{MUX.O}$ through the multiplexer and the one among the input signals $v_{DB.ENT}$ to $v_{DR.PVBAT}$ that the pin v_{DR} drives in the test mode.

The signals T_1 and T_2 set the mode of operation between normal, heavily sourced test mode, battery-assisted test mode and manual test mode. Here in the normal mode the circuit operates independent of the test signals, in the heavily sourced test mode circuit is set to operate only in heavily sourced region and in the battery-assisted test mode circuit is set to operate only in battery-assisted mode irrespective of the loading condition. In the manual test mode the circuit is not functional as a system but instead v_{DR} drives each separate block depending on the T_3, T_4, T_5 and T_6. However the monitoring of the signals is possible in each mode via the test multiplexer.

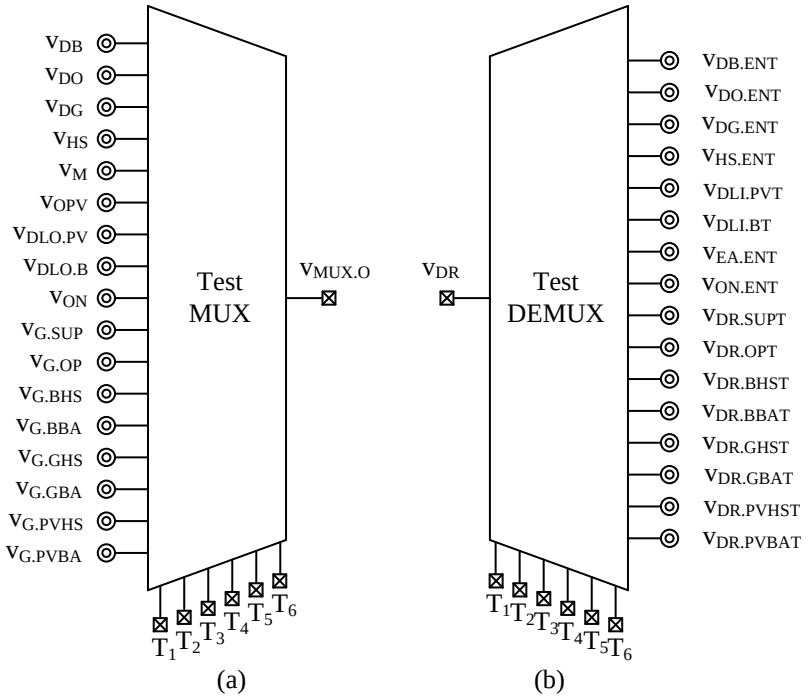


Fig. 6.10. Integrated test circuits (a) multiplexer (b) .de-multiplexer.

The test multiplexer is useful in evaluating the digital signals but evaluation of analog signal without affecting the integrity of the signals requires analog buffer that are larger in area. One solution to this problem is to use test pads, Fig. 6.11a. Test pads are roughly 10 × 10-μm^2 top metal plates that can lie on top of the circuits themselves. During the operation, to evaluate a particular signal, probes from a probe station can drop onto the test pads to measure the signal. The probes themselves add capacitance therefore this methods affects signal integrity but consume less area.

The integrated circuit design depends on the process models that model the different devices such as MOSFETs, capacitors and resistors. The difference between the models and actual fabricated-hardware can lead to loss in performance. In the process sensitive blocks, after characterizing the hardware, the programmable test circuits can

alter the device dimensions to shift the performance of the block to the desirable value. In bigger systems the selection is made by setting bits in the on board programmable memories. However in the harvesting system the more area effective solution is to implement metal fuses, Fig. 6.11b.

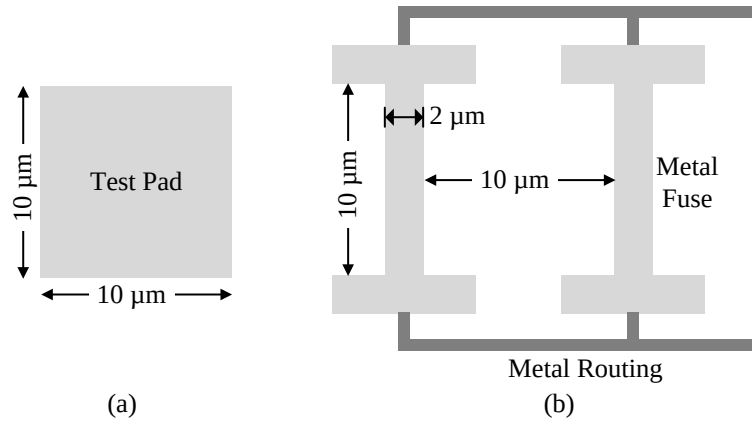


Fig. 6.11. Integrated test implementation (a) test pads (b) metal trims.

For example in the output diode comparator Fig. 5.11 trimming the relative size of M_6 and M_7 can help in tripping the comparator exactly at the inductor currents zero crossing. M_6 and M_7 have few of their fingers that connect through the 10×2 µm^2 top metal connection in Fig. 6.10b, blowing up the metal fuse with help of laser open the corresponding finger and shifts the comparator offset. The size of the metal fuse depends on the resolution of the laser and the number of fuse depends on the variation in adjustable parameter and available die area.

6.3.2 Energy Management

The major control blocks in the design, in Fig. 5.1, are error amplifier G_{BA}, battery-assist comparator CP_{BA}, heavily source comparator CP_{HS}, mode-detect comparator CP_M, photovoltaic comparator CP_{PV} and the diode comparators CP_O, CP_G and CP_B. The power

switches in this design are M_{PV}, M_G, M_{G1}, $M_{O(SUP)1}$–$M_{O(SUP)2}$, M_B and $M_{O(AID)}$. As already mentioned in Chapter 5, selected switch dimensions balance ohmic, gate-drive and control losses across P_{PV} and P_{LD}. Table 6.2 shows the contribution of different blocks in HS and BA mode.

Table 6.2. Energy and power loss distribution for reversing implementation

Blocks	Energy per Cycle [pJ]	Average Power [µW]
CP_M	9.7	0.63*
CP_{PV}	8.3	0.54*
Heavily Sourced (when P_{PV} = 70 µW and P_{LD} = 35 µW)		
CP_{HS}	8.6	0.56
CP_O	12	0.77
CP_B	8.4	0.55
$R_{ESR.L}$	24	1.56
Switches	85	5.55
Battery-Assisted (when P_{PV} = 70 µW and P_{LD} = 5 mW)		
G_{BA}	69	3.6*
CP_{BA}	128	6.7*
CP_O	12	0.62
CP_G	44	2.28
$R_{ESR.L}$	1950	101
Switches	2740	142

*Estimated

With the PV power at 70 µW and load at 35 µW the switches burn only 5.55 µW proportional to the power to power in transfers Similarly the switches proportionally higher power of 142 µW while transferring battery-assistance to the a 5mW load. And with 1 Ω of equivalent series resistance, L_X's $R_{ESR.L}$ burns 101 µW when battery-assisted and 1.56 µW when heavily sourced. In this prototype with the fixed PV and battery packets most of the losses scale with the input power

6.3.3 Power-Conversion Efficiency

The power conversion efficiency is the ratio of output power P_O and input power P_{IN}. In HS mode the P_O is the sum of P_{LD} and P_{BAT} and P_{IN} is P_{PV}. In BA mode, the sum of P_{PV}

and P_{BAT} sets P_{IN} and, P_{LD} defines P_O. Fig. 6.12 shows efficiency for 3 × 3 × 1.5 mm^3 and the Fig. 6.13 1.6 × 0.8 × 0.8-mm^3 inductors across P_{PV} 10–130 µW and P_{LD} upto 10 mW. As a fixed E_{PV} packet incurs a fixed current profile loss and, fixed switching action the ohmic losses and gate-drive losses scale with P_{PV} and efficiency remains constant across P_{PV}.

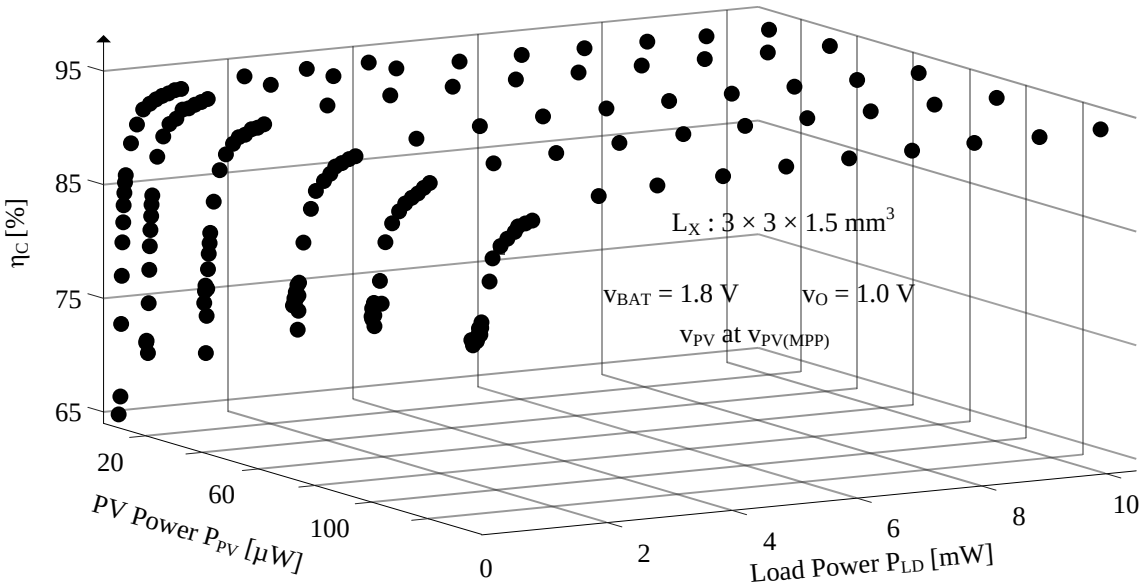


Fig. 6.12. Measured power-conversion efficiency across load and PV power for 3×3×1.5-mm^3 inductor.

The $R_{ESR.L}$ for the smaller inductor is 2 Ω and for the larger inductor is 1Ω. The quiescent losses of always-on blocks at offset the efficiency at low power level. By delivering multiple optimum-sized E_{BAT} the BA mode losses scale with P_{LD} and efficiency always flattens to a constant maximum value of 94.5 % and 88% for the different inductors as Fig. 6.12 and 6.13 shows. The switch loss of the $M_{O(AID)}$ switch that doesn't scale with load power causes the slight slope in the flat region of the efficiency

plots. Overall, the efficiency is 64%–94.5 % for the larger size L_X and 54%–88% for smaller size L_X across P_{PV} and P_{LD}.

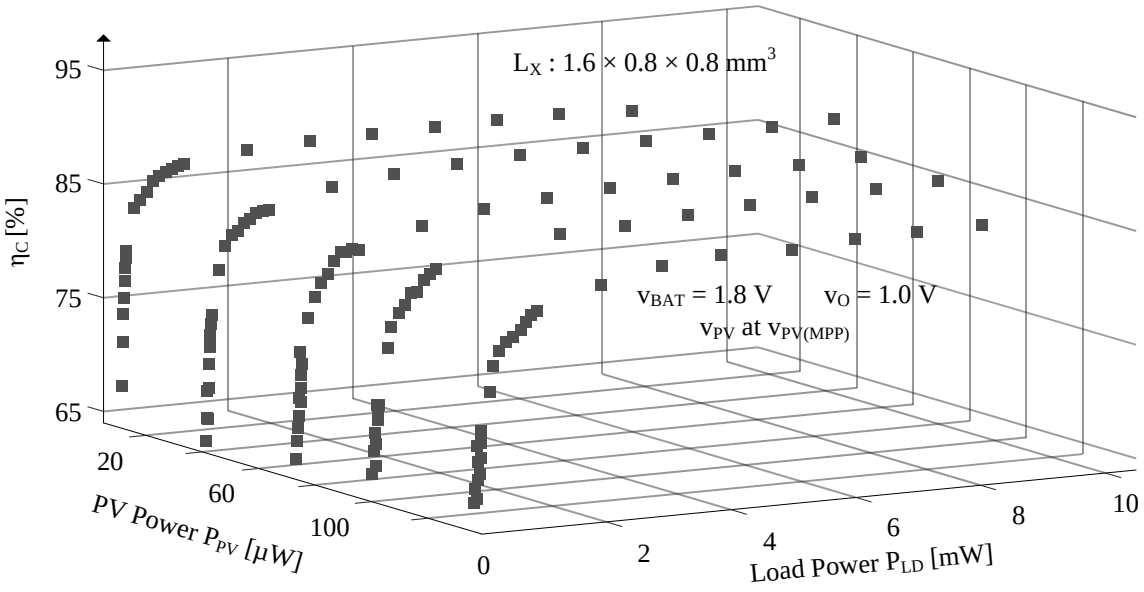


Fig. 6.13. Measured power-conversion efficiency across load and PV power for 1.6×0.8×0.8-mm^3 inductor.

6.4 Comparison and Assessment

6.4.1 Figure of Merit

The charger-supply system needs to occupy minimum footprint, transfer power with maximum efficiency and regulate the output voltage tightly about the reference voltage. The small footprint reduces the amount of materials used and thereby by reduces cost when millions of these sensors occupy a large infrastructure [1]–[20]. Smaller size sensors are also less invasive to the surrounding and therefore more of these sensors can spread across an area leading to more effective sensing and reporting of information [8]. In the charger supply system the main contributors to the volume are the IC, PV cell, and

the passives that include the input capacitor, output capacitor and the energy transferring inductors or capacitors. Stacking the PV cell at the top level, IC at the second level, and the passive at the third level allows for dense packing of the different components in a given volume [108]. The application space and technology decides the PV cell and the load level decides the size of the IC. So the challenge is to reduce the size of the passives [47]. A larger size inductor as Section 6.3 shows can have lower ESR and higher efficiency but increase footprint. Therefore the size of the inductor is in the denominator of the figure of merit:

$$\mathrm{FoM} = \left(\frac{\Delta i_{LD}}{C_O \Delta v_O} \right) \frac{\eta_{C(PK)}}{L_{X.VOL}}. \tag{6.4}$$

An accurate output voltage allows for increasing the noise margins for the sensor data transmissions and reliability of its analog circuit [1], therefore the output ripple Δv_O finds itself in the denominator of FoM. Most of the charger–supply circuits supply energy only periodically, but the load can continually discharge the output therefore an output capacitor is necessary to supply the load in phases of no energy transfer [100]–[116]. The size of capacitor is directly dependent of how fast the system can react to the a particular load step, as a result the ratio of the load step Δi_{LD} and capacitance C_O is higher for a superior compact system with faster response time. In other words the system with a large ratio of Δi_{LD} and C_O can accommodate a smaller capacitor and save space for a similar load step [38]. Efficiency is extremely important as the power transferred is only hundreds of microwatts from the PV cell and few milliwatts from the battery, an inefficient system can loses most of if not all the power across it and starve the sensor load [113]–[121].

6.4.2 Alternatives and Assessment

6.4.2.1 Non-Reversing and Reversing Comparison

Fig. 6.14 compares the efficiency of the non-reversing in Fig. 5.1 and reversing circuit in Fig. 5.18 across PV power. The non-reversing circuit uses a 47-µH 3 × 3 × 1.5 mm^3 inductor and the reversing circuit uses an 18-µH 3 × 3 × 1.5 mm^3 inductor or a 22-µH 1.6 × 0.8 × 0.8-mm^3. For the non-reversing circuit the efficiency varies between 63%–78% as the PV power varies between 10–100 µW. And for the reversing circuit the efficiency varies between 65%– 81% for the larger size L_X and 54%–70% for smaller size L_X across 10–130 µW P_{PV}. The power flow method in both the circuits for transferring PV power to load is same, however the reversing circuit employs variable switch sizing and input-offset for diode comparators. As a result the efficiency of the reversing circuit using similar size inductor is higher than the non-reversing implementation.

Fig. 6.15 compares the efficiency of non-reversing and reversing circuits across the load power. For the non-reversing circuit the efficiency varies between 73%–86% as the load power varies between 10 µW–1 mW for 100-µW PV power. And for the reversing circuit the efficiency varies between 78%–94.5% for the larger size L_X and 66%–88% for smaller size L_X across 10 µW–10 mW for 100-µW PV power. The reversing implementation employs variable switch sizing, better control circuit design and transfers multiple battery packet in comparison with the reversing circuit. As a result the reversing circuit's efficiency is higher especially as P_{LD} scales high.

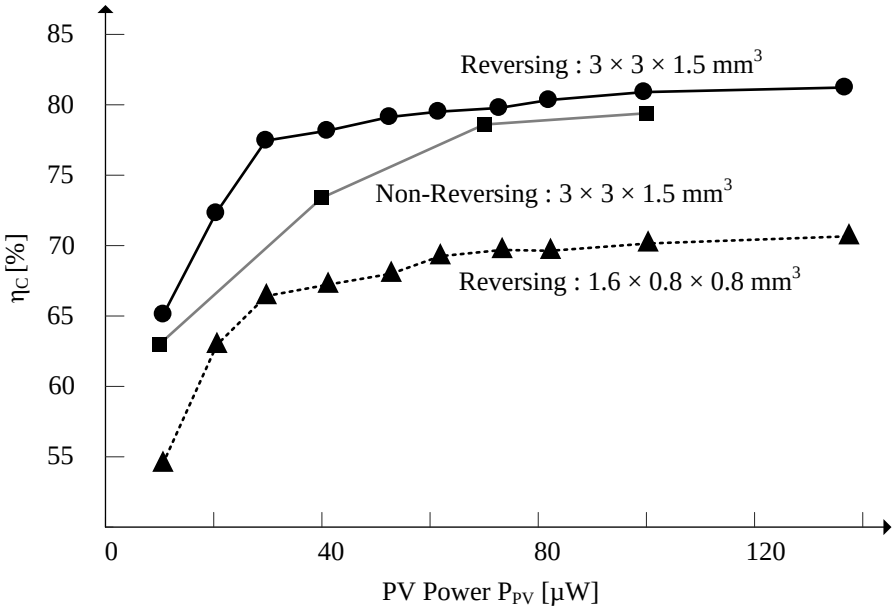


Fig. 6.14. Comparison between non-reversing and reversing circuits across PV power.

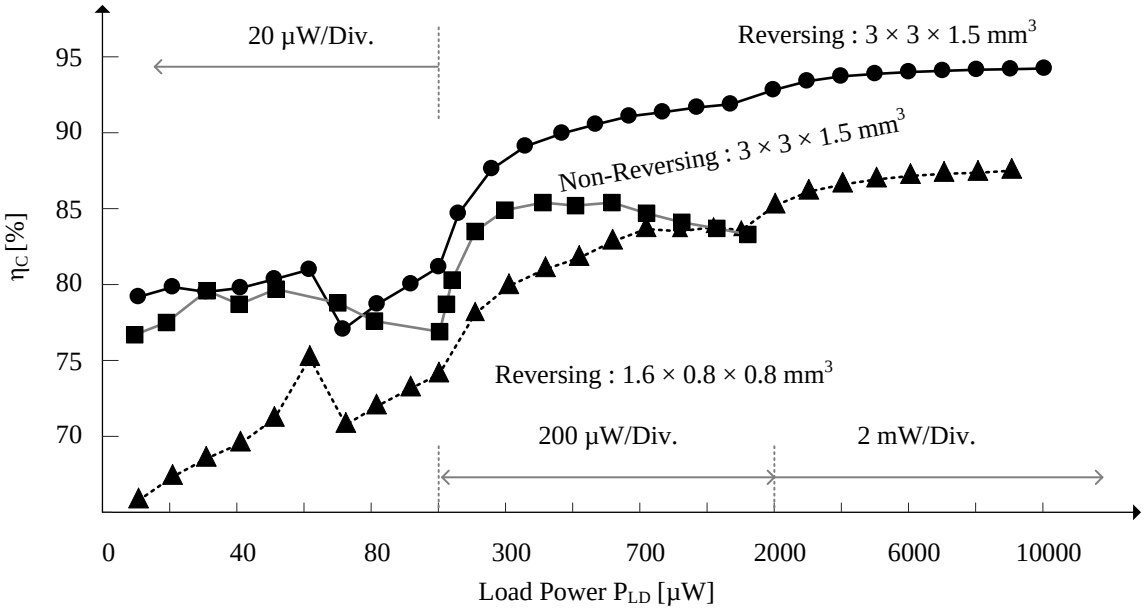


Fig. 6.15. Comparison between non-reversing and reversing circuit across load power.

6.4.2.2 Comparison with other Photovoltaic Charger–Supplies

In the state of the art charger–supply implementations the switched inductor and switched capacitor supplies are the two prominent options as Chapter 3 shows. The charger-supply

systems reuse the same power stage to charge the battery and supply the load. In charger–supplies, part or all of the PV energy, can directly be transfer to the load.

Switched Capacitor Charger–Supply: The charger–supply system in Fig. 6.16 uses the same switched-capacitor network (SCN) to draw power from the PV cell and battery to supply a load and recharge the battery. [108] implements an eight stage SCN using seven 45 pF MIM capacitors (C_{FLY}) to down convert 3.6-V in steps of 450 mV to supply a 0.45-V load. If the PV cell under the lighting conditions has an open-circuit voltage higher than 0.45 V then the system connects the PV cell to the 0.45 V node of the SCN via switch S_{CON}. This way PV cell can directly provide power to load. Also, since the SCN is bidirectional any excess power that the load doesn't consume flows into the battery. Similarly, if PV power is insufficient, and load voltage drops below 0.45 V, the SCN network down converts power from the battery to supply the load. If the open circuit voltage of PV cell drops below 0.45 V, it acts as load in the SCN network, as a result, S_{CON} disconnects the cell. Unfortunately, the voltage across the PV cell is kept at 0.45 V, but the optimum voltage across the PV cell that produces maximum power varies with light; therefore this method doesn't harness maximum power from PV cell under all light conditions.

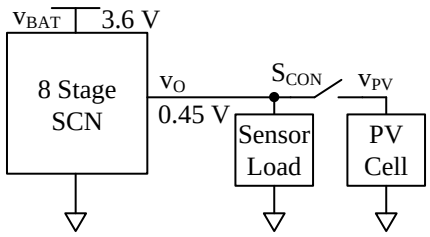


Fig. 6.16. Switched-capacitor charger–supply [108]

The switched-capacitor charger network in [107] and charger–supply network [108] from Tables 6.3 occupy less than 1 mm^2 of silicon area to draw and output less than 10 μW with 35%–50% efficiency, to implement fully integrated systems but at the cost of lower output power.

Single-Inductor Multiple-Output Charger–Supply: Single inductor multiple-input multiple-output power stages [102]–[104], [108]–[111], [113], [115]–[116] and [121] can viably charge a battery and supply a load by essential time-sharing the same inductor over a switching period. In the context of PV harvesting systems prior research in [109] and [110] shows simulation of systems that use a single inductor and a 6×6 cm^2 PV cell to harvester milliwatts of power. The work in [115] prototypes a PV harvester charger–supply that uses a 12 × 12 mm^2 inductor to draw power from 15–40 cm^2 PV cell to supply a load and charge a battery. The system operates in DCM and sends energy packets from the PV cell and battery to meet load requirements. The system harvests maximum power from the PV cell under varying lighting conditions by drawing appropriate size energy packets at a fixed frequency. When PV power is higher than P_{LD} sending PV energy packets to the output raises v_O. After vo rises to a reference voltage the system redirects packets to v_{BAT}, until load discharges v_O below the reference. When PV packets flow into the output, if v_O doesn't rise to the reference voltage in 8 clock cycles, the controller interprets P_{LD} is higher than P_{PV} and sends battery packets to v_O to recover it to the reference voltage. Here, the count of eight packets is a tradeoff between large drop at v_O before battery recovers it, and drawing power from battery when PV cell itself can meet the load requirement.

The system in [111] uses a 20-µH, low ESR inductor switching at 31.25 kHz to deliver 0.5–10 mW at a power-stage peak efficiency of 83%. In the context of millimeter scale harvesting systems, the low ESR inductor increases the size of the system, and scaling down the inductor size while sending large energy packets reduces efficiency. Another disadvantage is that, the system discharges v_{BAT} even when PV cell itself can satisfy P_{LD}, causing a double efficiency. [70] uses a 1-mH external inductor to charge a battery from an equivalent PV source at 60%–87% efficiency while transferring 5 µW – 10 mW power. The charger circuits [70] and [107] need a follow up power stage to supply a load that incurs additional cost in efficiency and components. The single inductor charger–supply system in [111] is appealing as it reuses the inductor and shows 83% peak efficiency but system size is much larger in the centimeter scale.

The 2nd prototyped IC's efficiency is 8.5 % higher than the 1st prototyped IC [102] that scales the size of battery packet and implements a 6 switch topology. The power-conversion efficiency of the switched inductor in [103] non-reversing charger–supply and [104] reversing charger-supply is relatively high at 68%–83% and 40%–87%, by switching at low frequency and thereby reducing quiescent losses, the tradeoff for this is output regulation, because with low frequency, output ripple grows with load current. In both [103] and [104] the robustness of the control method especially how the system avoids the interruption of the PV loop which supplying from battery is not clearly shown [104] draws picowatts of quiescent power and all the control blocks remain on continuously, and as a result the efficiency of this scheme does not scale as power increases. The 80%–95% efficient 3-switch topology in [119] can only buck from v_{PV} therefore need multiple PV cells and takes multiple transfers through a 20-mΩ ESR

bulky inductor to transfer from v_{PV} to v_{BAT}. As a result this circuit is not suitable for small footprint higher ESR inductors.

The ratio of efficiency and inductor size sets the FoM calculation in Table 6.3, as for a similar switching frequency Δv_O is fixed for given Δi_{LD} and C_O. Considering the regulation performance, efficiency and size of the passives, the 2nd prototype performs 13× better than the 1st prototype and 80 × better than the closest state of the art, Table 6.3. Table 6.3 further shows the comparison of prototyped ICs with PV chargers, even though the FoM is not valid for the chargers the prototyped ICs show higher efficiency while using inductors of smaller size.

In the 2nd prototype the multiple packet optimum efficiency battery power transfer, automatic mode control that lends itself to variable switch sizing for the different energy packets, the novel sequencing of battery packets between PV packets and as a result reduction of switching loss with the reuse of the ground switch all contribute towards the superior FoM.

Table 6.3. Performance summary and comparison with state of the art circuits.

	PV Chargers		PV Charger-Supplies					
	ISSCC '14 [107]	**ISSCC '11 [70]**	**TCAS '13 [108]**	**JSSC '15 [103]**	**JSSC '16 [119]**	**JSSC '16 [104]**	**1st IC [102]**	**2nd IC**
Power Stage	Switched C	Switched L	Switched C	Switched L	Switched L	Switched L	Switched L	Switched L
Tech. [µm]	0.18	0.25	0.18	0.18	0.5	0.18	0.18	0.21
v_{BAT} **[V]**	4	3	3.6	3	3.3	3.0	1.8	1.8
PV Cell	0.84	Emulated	0.07	24 × 1.6	24 × 31		3 × 3 × 1	1 ×1 × 1 mm^3
v_{PV} **[V]**	0.14–0.5	0.5–2	0.44–0.5		1.5–5.5	0.14–0.62	0.27–	0.42–0.46
Δv_{PV} **[mV]**				10	20		30	30
P_{PV} **[W]**	< 10 µ	< 10 m	< 80 n	< 100 µ	40 µ	50 n–1 µ	< 100 µ	10–140 µ
v_O **[V]**	—	—	0.45	1, 1.8	1–3.3	1	1	1
Δv_O **[mV]**	—	—		∝ i_{LD}	–66/33		–24/+25	–28/+28
$\Delta v_{O,LD}$ **[mV]**	—	—			–66/33		–75/+77	–72/+60
P_{LD} **[W]**	—	—	72 p–90 n	1 µ–10 m	0–20 m		0–1 m	0–10 m
t_R **[s]**	—	—					2.5 m	100 µ
L_X **[mm³]**	—	1 mH	—	10 µH, 5.8 × 5.2 × 4.5	4.7 µH, 20 mΩ 5.7 × 5.7 × 3*		47 µH, 2 Ω 3 × 3 × 1.5	18 µH, 1 Ω 3 × 3 × 1.5 (22 µH, 2 Ω 1.6 × 0.8 × 0.8)
C_{IN} **[F]**					4.7 µ		220 n	100 n
C_O **[F]**				10 µ	10 µ		2.2 µ	10 µ
f_{CLK} **[kHz]**	500 Hz–19 MHz		100	< 20			8–85	8–90
P_Q **[W]**	170 p–3 n	2.4–3.5 µ		< 400 n	2.8 µ	3.2 n	3–30 µ	3–66 µ
η_C	35%–50%	60%–87%		68%–83%	80%–95%	40%–87%	63%–86%	65%–94.5% (54%–88%)
FoM (Normalized)				×0.09	×0.138		×0.91	1 (×12.1)

*Estimated

6.5 Research Contributions

6.5.1 Efficient CMOS PV Cells

For harvesting light energy this work reuses the low cost single-well CMOS technology that fabricates the circuits to implement the PV cell, Chapter 2. This research implemented and compared the possible CMOS PV cell options in a single-well CMOS technology and proved harnessing power using the P^+ in N well top junction harnesses only 20% of the total energy that both the P^+ in N well junction and N well in substrate junctions can harness together. The research also proposed the configuration that opens the P^+ terminal to combine the shallower and deeper junctions while eliminating one top-surface metal connection from the structure, so more light can penetrate to generate even more power. Even though top junction only PV cell can isolate and accommodate multiple PV cells and circuits in the same die, it is normally undesirable. Since microsystems can only avail a few millimeters, dedicating one die to the PV cell and stacking it above the CMOS circuit produces much more power than placing the PV cell alongside the circuit. The study also revealed stacking PV cells are inefficient due to parasitic substrate leakage losses. Therefore this research proposes and uses a single CMOS PV cell as the transducer to harness light.

- R.D. Prabha and G.A. Rincon-Mora, "Drawing the Most Power from Low-Cost Single-Well 1-mm^2 CMOS Photovoltaic Cells," *IEEE Trans. on Circuits and Systems II* , vol. 64, no. 1, pp. 46-50, Jan. 2017.
- R.D. Prabha and G.A. Rincon-Mora, “CMOS photovoltaic-cell layout configurations for harvesting microsystems,” *IEEE Int. Midwest Symp.Circuits Syst.*, pp. 368-371, Aug. 2013.

6.5.2 Comparison of Harvesting Circuits for Tiny PV cells

To identify the power stage that can transfer the most amount power from a tiny on-chip PV cell, the research compared the switched-inductor and switched-capacitor circuits while transferring similar power levels. To maximize harvested output power, the circuit should be efficient, which is to say it should transfer and condition power by switching an in-package inductor. Still, Ohmic losses P_R are dominant and proportional to P_{PV}, with controller quiescent power P_Q not far behind and gate-charging losses P_G further back. Interestingly, capacitor-based circuits consume more power because they conduct higher RMS currents. Moreover, on-chip implementations lose additional power in charging and discharging parasitic bottom-plate capacitors. In other words, switched-inductor harvesters harness more light energy from chip-sized PV cells than switched-capacitor circuits, which is especially important when P_{PV} is low, cloud cover and artificial lighting conditions persist, and unobtrusiveness (i.e., integration) is imperative.

- R.D. Prabha, G.A. Rincon-Mora, and S. Kim, "Harvesting circuits for miniaturized photovoltaic cells," *IEEE Int. Symp. Circuits Syst.*, pp. 309-312, May 2011.

6.5.3 Design of Charger–Supply Circuits

This work showed how to design low-loss battery-assisted photovoltaic-sourced CMOS charger–supplies. And that non-reversing switched inductors are less lossy than the reversing counterparts when the output voltage is greater than the battery voltage, and *vice versa* otherwise. Headroom, dead-time currents, and reverse-current protection dictate which and how FETs should switch the network. Unidirectional switches that

conduct dead-time currents in the same direction can be diodes or diode-emulating FETs. But as inductor resistance and losses climb, the benefits of low-loss CMOS choices diminish. In these cases, switches can be more lossy, and as such, occupy up to 80% less silicon area.

- R.D. Prabha and G.A. Rincon-Mora, "How to Design Battery-Assisted Photovoltaic Switched-Inductor CMOS Charger–Supplies," *IEEE Int. Symp. Circuits Syst.*, May 2017.

6.5.4 Automatic Mode Switching and Battery-Assisted Control

A millimetre scale photovoltaic cells can provide only around 100 µW of power even in direct sunlight. However the sensor load can draw milliwatts of power while receiving and transmitting data. In the scenario that sensor needs more power than the PV cell the system has to draw assistance from battery to satisfy the sensor load. The automatic mode control proposed in this work monitors load condition to decide when to draw battery-assistance to supply the load and when to charge the battery with excess PV power. This way favours single energy transfer from PV cell to load and draws battery energy only when required. This work further showed that interleaving PV packet with a variable size battery packet that satisfies the load, can simultaneously draw power from PV cell and assistance from battery to satisfy the load. Unlike state of the art clocked systems that interrupt the flow of PV or battery packets to send the other, this method allows for a more robust system that doesn't interrupt the PV or output control loops while transferring power. The uninterrupted flow of PV packets also maximizes the power that

the system can draw from PV cell as any power that PV capacitance stores without being drawn can be lost across the PV diode.

- R.D. Prabha and G.A. Rincon-Mora, “0.18-um Light-Harvesting Battery-Assisted Charger-Supply CMOS System,” *IEEE Trans. on Power Electronics*, vol. 31, no. 4, pp. 2950–2958, Apr. 2016.
- R.D. Prabha and G.A. Rincon-Mora, “Battery-assisted and photovoltaic-sourced switched-inductor CMOS harvesting charger-supply,” *IEEE Int. Symp. Circuits Syst.* , pp. 253-256, May 2013.

6.5.5 Maximizing Power-Transfer Efficiency for Switched-Inductors

This research investigated and compared transferring fixed-frequency variable-size energy packets and fixed-packet-size variable-frequency. The loss analysis study conducted in this research identified that for millimeter scale inductor power stage, transferring fixed-peak current optimal energy packets and varying the frequency is constantly more efficient than state of the art schemes that vary the packets size while sending them out at fixed frequency. This work further proposed how to design switches, the controller and size the energy packet to maximize power transfer efficiency. And with a constant peak current, switch dimensions are optimal for all power levels. This way, microwatt power supplies can sustain more functions and tiny energy-harvesting microsystems can output more power.

- R.D. Prabha and G.A. Rincon-Mora, "Maximizing Power-Transfer Efficiency in Low-Power DC-DC Converters," *IET Electronic Letters*, vol. 51, no. 23, pp. 1918–1920, Nov. 2015.

6.5.6 Maximally Efficient Control

The first prototype in the research implements a fixed energy packet variable frequency control scheme that maximizes efficiency of power transfer from PV cell and load using the traditional 6 switch non-reversing power stage. In the prototype the battery power transfer uses a variable packet size scheme which is inefficient. To improve the efficiency of the battery power transfer, the second prototype proposes a new multiple fixed energy packet scheme, where the circuit provides multiple battery packets in between each PV packets. The multiple battery packet transfer scheme as a result achieve high and near constant efficiency across load power

The maximally efficient multiple battery packet control ensures priority for PV packet transfer and avoids condition where systems interrupts PV loop to send battery packets. The PWM loop that regulates the output during battery-assistance reduces the ripple across the load when higher power more noise sensitive analog blocks turn on. The research studied the different power stages available in literature and improves on the reversing charger–supply circuit in literature by replacing NMOS output switches with PMOS output switches and implementing a new switch sequencing to reduce gate-drive losses. The new switch-sequencing scheme aligns switching action in the reversing circuit to share the ground switch turn on time such that there is only on switching event while transferring a PV and a battery packet unlike literature that requires two.

The mode segregating control scheme allows for separation of high power battery-assistance mode and low power heavily sourced mode and as a result lends the power stage to use variable switch size of different modes unlike the state of the art

which uses a single switch size for both transfers. The robust control method and duty-cycled control circuits that implement them allows for higher PV frequency and as a result lower input capacitance. In the second prototype using the photovoltaic voltage to set the PV frequency also helps to avoid quiescent power consuming oscillator used in most state of the arts.

- R.D. Prabha and G.A. Rincon-Mora, "10-mW 94% Efficient 0.18-µm Battery-Assisted PV-Harvesting Charger–Supply," [*to be submitted to ISSCC 2018*]

- R.D. Prabha and G.A. Rincon-Mora, "10-mW 94% Efficient 0.18-µm Battery-Assisted PV-Harvesting Charger–Supply," [*To be submitted to JSSC*]

Table 6.4. Main contributions

	Description of main contributions
1	Implementation of a millimeter-scale single-inductor light-harvesting battery-assisted charger–supply system that can harvest efficiently from indoor to solar lighting conditions.
2	New CMOS PV cell configuration that can harvest more power.
3	Identification of power transfer scheme that maximizes harvesting efficiency.
4	Automatic mode switching and mode based variable switch sizing
5	Novel power transfer scheme that improves battery-supplying efficiency.

The research so far has generated four conference publications and four journal papers. A TPE journal paper is in the submission pipeline.

Peer-Reviewed Journals

- R.D. Prabha and G.A. Rincon-Mora, "10-mW 94% Efficient 0.18-µm Battery-Assisted PV-Harvesting Charger–Supply," [*To be submitted to TPE*]
- R.D. Prabha and G.A. Rincon-Mora, "Drawing the Most Power from Low-Cost Single-Well 1-mm^2 CMOS Photovoltaic Cells," *IEEE Trans. on Circuits and Systems II* , vol. 64, no. 1, pp. 46-50, Jan. 2017.

- R.D. Prabha and G.A. Rincon-Mora, “0.18-um Light-Harvesting Battery-Assisted Charger-Supply CMOS System,” *IEEE Trans. on Power Electronics*, vol. 31, no. 4, pp. 2950–2958, Apr. 2016.
- R.D. Prabha and G.A. Rincon-Mora, "Maximizing Power-Transfer Efficiency in Low-Power DC-DC Converters," *IET Electronic Letters*, vol. 51, no. 23, pp. 1918–1920, Nov. 2015.
- R.D. Prabha, D. Kwon, O. Lazaro, K.D. Peterson, and G.A. Rincon-Mora, “Increasing Electrical Damping in Energy-harnessing Transducers,” *IEEE Trans. Circuits and Systems II*, vol.58, no. 12, pp. 787-791, Dec. 2011.

Conferences

- R.D. Prabha and G.A. Rincon-Mora, “How to Design Battery-Assisted Photovoltaic Switched-Inductor CMOS Charger–Supplies,” *IEEE Int. Symp. Circuits Syst.*, May 2017.

- R.D. Prabha, G.A. Rincon-Mora, and S. Kim, “Harvesting circuits for miniaturized photovoltaic cells,” *IEEE Int. Symp. Circuits Syst.*, pp. 309-312, May 2011.
- R.D. Prabha and G.A. Rincon-Mora, “CMOS photovoltaic-cell layout configurations for harvesting microsystems,” *IEEE Int. Midwest Symp.Circuits Syst.*, pp. 368-371, Aug. 2013.
- R.D. Prabha and G.A. Rincon-Mora, “Battery-assisted and photovoltaic-sourced switched-inductor CMOS harvesting charger-supply,” *IEEE Int. Symp. Circuits Syst.* , pp. 253-256, May 2013.

6.6 Technological Limitations and Future Research Direction

To realize the ultimate aim of a standalone high efficiency low volume PV harvesting battery assisted charger–supply system few more functions needs to be implemented.

6.6.1 Maximum Power-Point Tracking

The Section 6.1 discusses the photovoltaic loop. This work manually controls the circuit to extract maximum power from the PV cell via the switching frequency in the 1st prototype and peak photovoltaic voltage in the 2nd prototype. The future research direction in this regard is to integrate the rest of the maximum power tracking circuits. For example in the case of the 2nd prototype an offset-fractional open circuit voltage can set the control signal v_{MPP} for this circuit can open the PV cell once in a while measure open circuit voltage and adjust v_{MPP}. Another option is optimize v_{MPP} with respect to the output power. In heavily sourced mode for a fixed load higher number of PV packets reaching the battery indicates greater extraction of PV energy. Similarly minimizing the number of packets in the battery-assisted case also indicates higher PV power. A digital control loop can count the number of packets reaching or leaving the battery in either modes and adjust v_{MPP} to maximize or minimize them respectively.

6.6.2 Zero-Energy Start-up

Both the implemented prototypes rely on battery energy to start operation. However prolonged non exposure to light or exposure to heavy load can deplete the battery. The self-discharge of battery technologies like super-capacitor are particularly high. The circuit solution that can directly use PV energy to start switching can allow for startup from a depleted battery. Challenge here is the low voltage of the PV cell provides limited headroom for driving the main power stage. Literature presents self-oscillating circuits

[30] that helps to charge up a smaller energy buffer that act as temporary energy buffer and provides headroom to operate the main power stage. Integrating these circuits could be a possible solution to start from low battery energy. Another option that can be explored with CMOS PV cells is to configure a stack of PV cells for startup. For this the available PV area can divide into multiple cells that supply in parallel as one cell for high efficiency normal operations and some of them operate in series during startup to provide higher headroom

6.6.3 Battery Protection

The battery technologies operate properly within particular voltage bounds. For example charging a Li-ion battery above 4.2 V or discharging it below 2.7 V can destroy it permanently. To avoid this, a battery voltage comparator can monitor the battery voltage and stop energy transfer if the voltage drifts outside operation bounds. For example in heavily sourced mode one battery voltage reaches higher threshold the comparator stops more energy packets from reaching battery. Similarly the comparator shuts the off the load if the battery voltage drifts to the lower threshold.

6.6.4 CMOS cell Integration

In a purely energy harvesting application integrating the CMOS cell on the same die as circuit is undesirable. Since microsystems can only avail a few millimeters, dedicating one die to the PV cell and stacking it above the CMOS circuit produces much more power than placing the PV cell alongside the circuit, especially when drawing power from multiple junctions. However in imaging applications, CMOS imagers [54]–[55] use diodes to capture images, these diodes can be reconfigured to harvest energy and charge

battery during systems idle phase. The challenge here is the substrate is lowest potential for the imager circuits and as a result the substrate junction cannot participate in harvesting power. One future direction is to envision a power stage that can harvest from negative voltages.

The proposed power stage in Fig. 6.17 implements the functionality of the prototyped IC while harvesting from a negative voltage with one less switch. To transfer power from PV cell to v_O, first switches S_{PV} and S_G close to energize L_X from v_{PV}, S_{PV} then open and S_O closes to drain L_X to v_O. After satisfying the load, the circuit steers energy to the battery by first closing S_{PV} and S_G to energize L_X from v_{PV}, and opening S_{PV} closing S_{CH} to drain L_X to v_{BAT}. When load requires assistance from the battery, the circuit energizes L_X by connecting it across v_{BAT} and v_O via S_{PS} and S_O; S_O and S_G then drains L_X to v_O.

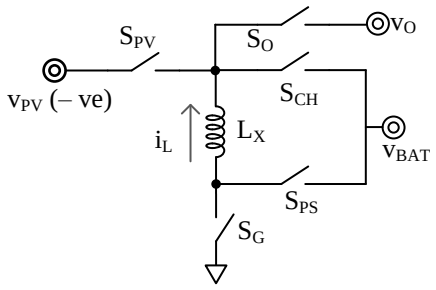


Fig. 6.17. Power stage integrating CMOS PV cell in same die.

6.7 Summary

This research investigated the design of a millimeter-scale single-inductor light-harvesting battery-assisted charger–supply system that can harvest efficiently from indoor to solar lighting conditions. The work developed, designed, simulated, fabricated and tested two prototype charger–supply systems (i) maximized the efficiency of the PV power path and (ii) additionally maximized the efficiency of the battery path as well. The

research also developed a CMOS PV cell that acted as the energy source in the second prototype. The research studied, evaluated and compared various power stage and power flow options and implemented new power stage and control scheme that provides 80 × improvements in figure of merit considering the regulation performance, efficiency and size of the passives.

REFERENCES

1. G. Chen, S. Hanson, D. Blaauw, and D. Sylvester "Circuit Design Advances for Wireless Sensing Applications, " *Proc. IEEE*, vol. 98, no. 11, pp. 1808-1827, Nov. 2010.

2. A. Shamim, M. Arsalan, L. Roy, and G. Tarr, "Wireless Dosimeter: System-on-Chip Versus System-in Package for Biomedical and Space Applications, " *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 55, no. 7, pp. 643-647, Jul. 2008.

3. L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas and H. Naas, "A very low-power CMOS mixed-signal IC for implantable pacemaker applications," *in IEEE J. of Solid-State Circuits*, vol. 39, no. 12, pp. 2446-2456, Dec. 2004.

4. M. M. Ahmadi and G. A. Jullien, "A Wireless-Implantable Microsystem for Continuous Blood Glucose Monitoring," in *IEEE Trans. on Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 169-180, June 2009.

5. T. Arampatzis, J. Lygeros, and S. Manesis, “A survey of applications of wireless sensors and wireless sensor networks,” *Proc. 13th Mediterranean Conference on Control and Automation*, Limassol, Cyprus, 2005, pp. 719-724.

6. Z. Tafa, G. Dimic, and V. Milutinovic, “A survey of military applications of wireless sensor networks,” *Embedded Computing (MECO)*, June 2012, pp. 196-199.

7. G. Nikolakopoulos, S. Manesis, “A survey on underwater wireless sensor networks and applications,” *Control & Automation (MED)*, July 2012, pp. 1147-1154.

8. B. W. Cook, S. Lanzisera, and K. S. J. Pister, "SoC Issues for RF Smart Dust, " *Proc. IEEE*, vol. 94, no. 6, pp. 1177-1196, Jun. 2006.

9. D. Puccinelli and M. Haenggi, "Wireless sensor networks: applications and challenges of ubiquitous sensing, " *IEEE Circuits Syst. Mag.*, vol. 3, no. 3, pp. 19-29, 2005.

10. M. Fojtik, D. Kim, G. Chen, Y. Lin, D. Fick, J. Park, M. Seok, M. Chen, Z. Foo, D. Blaauw, and D. Sylvester, "A Millimeter-Scale Energy-Autonomous Sensor System With Stacked Battery and Solar Cells, " *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 801-813, Mar. 2013.

11. G.P. Hancke, H. Madhoo, A. Khatri, “A survey of wireless sensor network applications from a power utility's distribution perspective,” *AFRICON*, Sep. 2011, pp. 1-5.

12. A. Rytter. “Vibration based inspection of civil engineering structures”, *PhD dissertation*, Dept. of Building Technology and Structural Eng., Aalborg University, Denmark, 1993.

13. A. Mainwaring, J. Polastre, R. Szewczyk, D. Culler, and J. Anderson, “Wireless sensor networks for habitat monitoring”, *ACM Inter. Workshop on Wireless Sensor Networks and Applications (WSNA'02)*, Atlanta, GA, 2002.

14. T. He, S. Krishnamurthy, J. A. Stankovic, T. Abdelzaher, L. Luo, R. Stoleru, T. Yan, L. Gu, J. Hui, B. Krogh, “An energy-efficient surveillance system using wireless sensor networks”, *MobiSys'04 Proceedings of the 2nd international conference on mobile systems, applications, and services*, 2004, pp. 270-283.

15. B. Sinopoli, C. Sharp, L. Schenato, S. Shaffert, Sh. S. Sastry, “Distributed control applications within sensor networks”, *Proc. of the IEEE*, August 2003, pp. 1235-1246.

16. A. Arora et. al., “A line in the sand: a wireless sensor network for target detection, classification, and tracking,” *Computer Networks, Military Communications Systems and Technologies*, vol. 46, no. 5, pp. 605-634, Dec. 2004.

17. Sachine Gajjar, “Factors influencing the wireless sensor network design,” *Proc. of the 2009 International Conference on Signals, Systems & Automation*, pp. 166-169, Apr. 2010.

18. A. L. Aita, M. A. P. Pertijs, K. A. A. Makinwa and J. H. Huijsing, "A CMOS smart temperature sensor with a batch-calibrated inaccuracy of ±0.25°C (3σ) from −70°C to 130°C," *IEEE Int. Solid-State Circuits Conference*, 2009, pp. 342-343.

19. S. Hanson and D. Sylvester, "A 0.45–0.7V sub-microwatt CMOS image sensor for ultra-low power applications," *Symp. on VLSI Circuits*, 2009, pp. 176-177.

20. R. Rofougaran, Tsung-Hsien Lin and W. J. Kaiser, "CMOS front-end LNA-mixer for micropower RF wireless systems," *Proc.. 1999 International Symposium on Low Power Electronics and Design*, 1999, pp. 238-242.

21. F. S. Lee and A. P. Chandrakasan, "A 2.5 nJ/bit 0.65 V Pulsed UWB Receiver in 90 nm CMOS," in *IEEE J. of Solid-State Circuits*, vol. 42, no. 12, pp. 2851-2859, Dec. 2007.

22. N. M. Pletcher, S. Gambini and J. Rabaey, "A 52 µW Wake-Up Receiver With –72 dBm Sensitivity Using an Uncertain-IF Architecture," in *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269-280, Jan. 2009.

23. D. D. Wentzloff and A. P. Chandrakasan, "A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS," 2007 *IEEE Int. Solid-State Circuits Conf.*, 2007, pp. 118-591.

24. U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE J. of Solid-State Circuits*, vol. 38, no. 10, pp. 1602-1608, Oct. 2003.

25. J. M. Rabaey et al., "PicoRadios for wireless sensor networks: the next challenge in ultra-low power design," *IEEE Int. Solid-State Circuits Conf.*, 2002, pp. 200-201 vol.1.

26. B. H. Calhoun, D. C. Daly, N. Verma, D. F .Finchelstein, D. D. Wentzloff, A. Wang, S. Cho, and A. P. Chandrakasan, "Design considerations for ultra-low energy wireless microsensor nodes, " *IEEE Trans. Computers*, vol. 54, no. 6, pp. 727-740, Jun. 2005.

27. B. A. Warneke, M. D. Scott, B. S. Leibowitz, L. Zhou, C. L. Bellew, J. A. Chediak, J. M. Kahn , B. E. Boser, and K. S. J. Pister, "An autonomous 16 mm3 solar-powered node for distributed wireless sensor networks, " *Proc. IEEE Sensors*, vol. 1, no. 2, pp. 1510-1515, Jun. 2002.

28. R.J.M. Vullers, R. van Schaijk, H.J. Visser, J. Penders, and C. Van Hoof, "Energy harvesting for autonomous wireless sensor networks, " *IEEE Solid-State Circuits Mag.*, vol. 2, no. 2, pp. 29–38, Spring 2010.

29. P.D. Mitcheson, E.M. Yeatman, G.K. Rao, A.S. Holmes, and T.C. Green, "Energy harvesting from human and machine motion for wireless electronic devices, " *Proc. IEEE*, vol. 96, no. 9, pp. 1457-1486, Sept. 2008.

30. A. Blanco and G.A. Rincon-Mora, "Energy-Harvesting Microsensors: Low-Energy Task Schedule & Fast Drought-Recovery Design," *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, 2016., pp. 1-4..

31. Cymbet Corporation, Rechargeable Thin Film Battery 12 μAh, 3.8 V, *EnerChip CBC012 datasheet*, 2009.

32. O. Lazaro. “CMOS Inductively coupled Power Receiver for Wireless Microsensors”, *PhD dissertation*, School of Electrical and Computer Eng., Georgia Tech, Atlanta, 2014.

33. S. Kim. “Mixed-source Charger-Supply CMOS IC”, *PhD dissertation*, School of Electrical and Computer Eng., Georgia Tech, Atlanta, 2014.

34. T. Christen and M. W. Carlen, “Theory of Ragone plots,” *Journal of Power Sources*, vol. 91, no. 2, pp. 210-216, Dec. 2000.

35. T. Christen and C. Ohler, “Optimizing energy storage devices using Ragone plots,” *Journal of Power Sources*, vol. 110, no. 1, pp. 107-116, July 2002.

36. D. Linden and T.B. Reddy, *Handbook of batteries*, 3rd ed., New York, NY:McGraw-Hill, 2002.

37. J. B. Bates, N. J. Dudney, et. al., “Thin-film lithium and lithium-ion batteries,” *Solid State Ionics*, vol. 135, pp. 33-45, Nov. 2000.

38. G.A. Rincon-Mora, *Power IC Design: Top-Down Approach*, 5th Edition, Raleigh: Lulu, 2009.

39. S. Priya and D.J. Inman, *Energy Harvesting Technologies*, New York, NY: Springer Science+Business Media, LLC 2009.

40. Y. K. Ramadass and A. P. Chandrakasan, "A Battery-Less Thermoelectric Energy Harvesting Interface Circuit With 35 mV Startup Voltage, " *IEEE J. Solid-State Circuits*, vol. 46, no.1, pp. 333-341, Jan. 2011.

41. E. O. Torres and G. A. Rincon-Mora, "A 0.7-µm BiCMOS Electrostatic Energy-Harvesting System IC, " *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 483-496, Feb. 2010.

42. D. Kwon and G. A. Rincon-Mora, "A Single-Inductor 0.35 µm CMOS Energy-Investing Piezoelectric Harvester, " *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2277-2291, Oct. 2014.

43. G. D. Szarka, B. H. Stark, and S. G. Burrow, "Review of Power Conditioning for Kinetic Energy Harvesting Systems, " *IEEE Trans. Power Electronics*, vol. 27, no. 2, pp. 803-815, Feb. 2012.

44. Na Kong and Dong Sam Ha, "Low-Power Design of a Self-powered Piezoelectric Energy Harvesting System With Maximum Power Point Tracking, " *IEEE Trans. Power Electronics*, vol. 27, no. 5, pp. 2298-2308, May 2012.

45. G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS Threshold-Compensated RF Energy Harvester, " *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985-1997, Sep. 2011.

46. S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1 nW Energy-Harvesting System with 544 pW Quiescent Power for Next-Generation Implants, " *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2812-2824, Dec. 2014.

47. R. D. Prabha, G. A. Rincon-Mora, and S. Kim, "Harvesting circuits for miniaturized photovoltaic cells, " *IEEE Int. Symp. Circuits Syst.*, pp. 309-312, May 2011.

48. R. J. M. Vullers, R. van Schaijk, I. Doms, C. Van Hoof, and R. Mertens, "Micropower energy harvesting, " *Solid-State Electronics*, vol. 53, no. 7, pp. 684-693, Jul. 2009

49. E.O. Torres and G.A. Rincón-Mora, "Long-lasting, self-sustaining, and energy-harvesting system-in-package (SiP) wireless micro-sensor solution, " *Int. Conf. on Energy, Environment, and Disasters*, pp. 1-33 , Jul. 2005.

50. S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes, " *Computer Communications*, vol. 26, no. 11, pp. 1131-1144, Jul. 2003.

51. A. Hande, T. Polk, W. Walker, and D. Bhatia, "Indoor solar energy harvesting for sensor network router nodes, " *Microprocessors & Microsystems*, vol. 31, no. 6, pp. 420-432, Sept. 2007.

52. A. Sinha and A. Chandrakasan, "Dynamic Power Management in Wireless Sensor Networks, " *IEEE Design & Test of Computers*, vol. 18, no. 2, pp. 62-74, Mar. 2001.

53. M.A. Green, *Solar Cells: Operating principles, Technology, and System Applications*, N.J.: Prentice-Hall, 1982.

54. M. L.Simpson, M. N. Ericson, G. E. Jellison, W. B. Dress, A. L.Wintenberg, and M. Bobrek, "Application specific spectral response with CMOS compatible photodiodes, " *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 905-913, May 1999.

55. R.J. Perry, "Analysis and characterization of the spectral response of CMOS based integrated circuit (IC) photodetectors, " *Proc. University/Government/Industry Microelectronics Symp.*, pp.170-175, 1999.

56. R. D. Prabha and G. A. Rincon-Mora, "CMOS photovoltaic-cell layout configurations for harvesting microsystems, " *IEEE Int. Midwest Symp.Circuits Syst.*, pp. 368-371, Aug. 2013.

57. M. Ferri, D. Pinna, M. Grassi, E. Dallago, and P. Malcovati, "Model of integrated micro photovoltaic cell structures for harvesting supplied microsystems in 0.35-µm CMOS technology, " *IEEE Sensors*, pp. 232-235, Nov. 2010.

58. S. Ghosh, H. Wang, and W.D. Leon-Salas, "A Circuit for Energy Harvesting Using On-Chip Solar Cells, " *IEEE Trans. Power Electronics*, vol. 29, no. 9, pp. 4658-4671, Sept. 2014.

59. •R.D. Prabha and G.A. Rincon-Mora, "Drawing the Most Power from Low-Cost Single-Well 1-mm^2 CMOS Photovoltaic Cells," *IEEE Trans. on Circuits and Systems II* , vol. 64, no. 1, pp. 46-50, Jan. 2017.

60. M. Baldauf, W. Preidel, "Status of the development of a direct methanol fuel cell", *Journal of Power Sources*, 1999, pp. 161-166.

61. A. Blum, T. Duvdevani, et. al., "Water-neutral micro direct-methanol fuel cell (DMFC) for portable applications", *Journal of Power Sources*, 2003, pp. 22-25.

62. C.Y. Chen, P. Yang, "Performance of an air-breathing direct methanol fuel cell", *Journal of Power Sources*, 2003, pp. 37-42.

63. C.W. Moore, J. Li, and P.A. Kohl, “Microfabricated fuel cells with thin-film silicon dioxide proton exchange membranes,” *Journal of the Electrochemical Society*, vol. 152, no. 8, pp. 1606-1612, Aug. 2005.

64. T.J. Yen, N. Fang, X. Zhang, G.Q. Lu, C.Y. Wang, “A micro methanol fuel cell operating at near room temperature,” *Applied Physics Letters*, vol. 83, no. 19, Nov. 2003.

65. M. Frank, M. Kuhl, et al., “An integrated power supply System for low-power 3.3 V electronics using on-chip polymer electrolyte membrane (PEM) fuel cells”, *Proc. IEEE Int. Solid-State Circuits Conf.* (ISSCC), pp. 292-293, Feb. 2009.

66. L. C. Olsen, P. Cabauy, and B. J. Elkind, “Betavoltaic Power Sources,” *Physics Today*, vol. 65, no. 12, pp.35-38, Dec. 2012.

67. M.A. Green, et al., “Solar cell efficiency tables (Version 50),” Prog. in Photovoltaics: Research and Applications, vol. 25, no. 7, pp. 668–676, 2017.

68. T. Esram and P. L. Chapman, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques, " *IEEE Trans. Energy Conversion*, vol. 22, no. 2, pp. 439-449, June 2007.

69. H.P. Forghani-zadeh and G.A. Rincon-Mora, "Current-sensing techniques for dc-dc converters," *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, vol. 2, pp. 577-580, 2002.

70. Y. Qiu, C. V. Liempd, B. O. Veld, P. G. Blanken, and C. V. Hoof, "5μW-to-10mW input power range inductive boost converter for indoor photovoltaic energy harvesting with integrated maximum power point tracking algorithm, " *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 118-120, Feb. 2011.

71. L. L. Buciarelli, B. L. Grossman, E. F. Lyon, and N. E. Rasmussen, "The energy balance associated with the use of a MPPT in a 100 kW peak power system", *IEEE Photovoltaic Spec. Conf.*, pp. 523-527, 1980.

72. J. D. van Wyk and J. H. R. Enslin, "A study of wind power converter with microprocessor based power control utilizing an oversynchronous electronic scherbius cascade", *Proc. IEEE Int. Power Electron. Conf.*, pp. 766-777, 1983.

73. W. J. A. Teulings, J. C. Marpinard, A. Capel, and D. O'Sullivan, "A new maximum power point tracking system", *Proc. 24th Annu. IEEE Power Electron. Spec. Conf.*, pp. 833-838, 1993.

74. Y. Kim and H. Jo, D. Kim, "A new peak power tracker for cost-effective photovoltaic power system", *Proc. 31st Intersociety Energy Convers. Eng. Conf.*, pp. 1673-1678, 1996.

75. O. Hashimoto, T. Shimizu, and G. Kimura, "A novel high performance utility interactive photovoltaic inverter system", *Conf. Record 2000 IEEE Ind. Appl. Conf.*, pp. 2255-2260, 2000.

76. A. F. Boehringer, "Self-adapting dc converter for solar spacecraft power supply", *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-4, no. 1, pp. 102-111, Jan. 1968.

77. E. N. Costogue and S. Lindena, "Comparison of candidate solar array maximum power utilization approaches", *Intersociety Energy Conversion Eng. Conf.*, pp. 1449-1456, 1976.

78. J. Harada and G. Zhao, "Controlled power-interface between solar cells and ac sources", *IEEE Telecommun. Power Conf.*, pp. 22.1/1-22.1/7, 1989.

79. K. H. Hussein and I. Mota, "Maximum photovoltaic power tracking: An algorithm for rapidly changing atmospheric conditions", *IEE Proc. Generation Transmiss. Distrib.*, pp. 59-64, 1995.

80. A. Brambilla, M. Gambarara, A. Garutti, and F. Ronchi, "New approach to photovoltaic arrays maximum power point tracking", *Proc. 30th Annu. IEEE Power Electron. Spec. Conf.*, pp. 632-637, 1999.

81. K. Irisawa, T. Saito, I. Takano, and Y. Sawada, "Maximum power point tracking control of photovoltaic generation system under non-uniform insolation by means of monitoring cells", *Conf. Record Twenty-Eighth IEEE Photovoltaic Spec. Conf.*, pp. 1707-1710, 2000.

82. A. M. Marzouk, A. A. Abdelmoaty, A. Helmy and Y. Ismail, "TPQA: Three point quadrature approximation MPPT algorithm," *IEEE Int. Conf. on Electronics, Circuits, and Systems (ICECS)*, 2013, pp. 397-400.

83. J. J. Schoeman, J. D. van Wyk, "A simplified maximal power controller for terrestrial photovoltaic panel arrays", *Proc. 13th Annu. IEEE Power Electron. Spec. Conf.*, pp. 361-367, 1982.

84. M. Buresch, Photovoltaic Energy Systems, New York:McGraw Hill, 1983.

85. G. W. Hart, H. M. Branz, and C. H. Cox, "Experimental tests of open-loop maximum-power-point tracking techniques", *Solar Cells*, vol. 13, pp. 185-195, 1984.

86. D. J. Patterson, "Electrical system design for a solar powered vehicle", *Proc. 21st Annu. IEEE Power Electron. Spec. Conf.*, pp. 618-622, 1990.

87. M. A. S. Masoum, H. Dehbonei, E. F. Fuchs, "Theoretical and experimental analyses of photovoltaic systems with voltage and current-based maximum power-point tracking", *IEEE Trans. Energy Convers.*, vol. 17, no. 4, pp. 514-522, Dec. 2002.

88. H.-J. Noh, D.-Y. Lee, D.-S. Hyun, "An improved MPPT converter with current compensation method for small scaled PV-applications", *Proc. 28th Annu. Conf. Ind. Electron. Soc.*, pp. 1113-1118, 2002.

89. K. Kobayashi, H. Matsuo, Y. Sekine, "A novel optimum operating point tracker of the solar cell power supply system", *Proc. 35th Annu. IEEE Power Electron. Spec. Conf.*, pp. 2147-2151, 2004.

90. B. Bekker, H. J. Beukes, "Finding an optimal PV panel maximum power point tracking method", *Proc. 7th AFRICON Conf. Africa*, pp. 1125-1129, 2004.

91. F. Horiguchi, "Integration of series-connected on-chip solar battery in a triple-well CMOS LSI," *IEEE Trans. Electron Devices*, vol. 59, no.6, pp. 1580–1584, Jun. 2012.

92. U. Cilingiroglu, B. Tar, and C. Ozmen, "On-Chip Photovoltaic Energy Conversion in Bulk-CMOS for Indoor Applications," *IEEE Trans. Circuits and Systems I*, vol. 61, no. 8 pp. 2491–2504, Aug. 2014.

93. Y. Ogasahara, *et al.*, "Supply Noise Suppression by Triple-Well Structure," *IEEE Trans. Very Large Scale Integration Systems*, vol. 21, no. 4, pp.781–785, Apr. 2013.

94. H. Lee, "Wideband characterization of a typical bonding wire for microwave and millimeter-wave integrated circuits," *IEEE Trans. Microwave Theory and Techniques*, vol. 43, no. 1, pp.63–68, Jan 1995.

95. C. Olalla *et al.*,"Architectures and Control of Submodule Integrated DC-DC Converters for Photovoltaic Applications," *IEEE Trans. on Power Electronics*, pp. 1 – 17, Sep. 2012.

96. A. Poruba , J. Springer a, L. Mullerova, A. Beitlerova , M. Vanecek, N. Wyrsch, and A. Shah, " Temperature dependence of the optical absorption coefficient of microcrystalline silicon," *J. of non-Crystalline Solids*, pp. 338-340, 2004.

97. Doug H. Rose, et al., "Fabrication Procedures and Process Sensitivities for CdS/CdTe Solar," Prog. in Photovoltaics: Research and Applications, no. 7, pp. 331–340, 1999.

98. D. Baderna, "Efficiency comparison between doubler and Dickson charge pumps, " *Int. Symp. on Circuits and Systems*, pp. 1891-1894, May 2005.

99. A. Pressman, *Switching Power Supply Design*, New York: McGrawHill, 1991.

100. R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd Ed., New York: Springer Science & Business Media, LLC, 2001.

101. R.D. Prabha and G.A. Rincon-Mora, "Maximizing Power-Transfer Efficiency in Low-Power DC-DC Converters," *IET Electronic Letters*, vol. 51, no. 23, pp. 1918–1920, Nov. 2015.

102. R.D. Prabha and G.A. Rincon-Mora, “0.18-um Light-Harvesting Battery-Assisted Charger-Supply CMOS System,” *IEEE Trans. on Power Electronics*, vol. 31, no. 4, pp. 2950–2958, Apr. 2016.

103. K. W. R. Chew, Z. Sun, H Tang, and L. Siek, "A 400nW single-inductor dual-input-tri-output DC-DC buck-boost converter with maximum power point tracking for indoor photovoltaic energy harvesting, " *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp.68-69, Feb. 2013.

104. D. El-Damak and A.P. Chandrakasan, “A 10 nW–1 μW Power Management IC With Integrated Battery Management and Self-Startup for Energy Harvesting Applications,” *IEEE J. of Solid-State Circuits*, vol. 51, no. 4, pp. 943–954, April 2016.

105. L. Su, D. Ma, and A.P. Brokaw, "Design and analysis of monolithic step-down SC power converter with subthreshold DPWM control for self-powered wireless sensors", *IEEE Trans. Circuits Syst. I*, vol. 57, no. 1, pp. 280-290, Jan. 2010.

106. D. Brunelli, C. Moser, L. Thiele, Member, and L. Benini., "Design of a Solar-Harvesting Circuit for Batteryless Embedded Systems," *IEEE Trans. on Circuits and Systems I*, vol. 56, no. 11, pp. 2519-2528, Nov. 2009.

107. W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, and D. Blaauw, "A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter, " *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 398-399, Feb. 2014.

108. M. H. Ghaed, G. Chen, R. Haque, M. Wieckowski, Y. Kim, G. Kim, Y. Lee, I. Lee; D. Fick, D. Kim, M. Seok, K. D. Wise, D. Blaauw, and D. Sylvester, "Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor, " *IEEE Trans.Circuits Syst. I: Regular Papers*, vol. 60, no. 12, pp. 3152-3162, Dec. 2013.

109. H. Shao, C. Tsui, and W. Ki, "A single inductor dual input dual output DC–DC converter with hybrid supplies for solar energy harvesting applications, " *Int. Symp. on Low Power Electronics and Design*, pp. 69–74, 2009.

110. H. Shao; C. Tsui; W. Ki, "A single inductor DIDO DC-DC converter for solar energy harvesting applications using band-band control, " *IEEE VLSI Syst. on Chip Conf.* , pp. 167-172, Sept. 2010.

111. S. Bandyopadhyay and A. P. Chandarkasan, "Platform Architecture for Solar, Thermal, and Vibration Energy Combining with MPPT and Single Inductor, " *IEEE J. of Solid-State Circuits*, vol. 47, no.9, pp-2199-2215, Sept 2012.

112. I. Chowdhury and D. Ma, "Design of Reconfigurable and Robust Integrated SC Power Converter for Self-Powered Energy-Efficient Devices, " *IEEE Trans. on Industrial Electronics*, vol. 56, no. 10, pp. 4018-4028, Oct. 2009.

113. Min Chen and G. A. Rincón-Mora, "Single inductor, multiple input, multiple output (SIMIMO) power mixer-charger-supply system, " *IEEE Int. Symp. Low Power Electronics and Design*, pp. 310-315, Aug. 2007.

114. R. D. Prabha and G. A. Rincon-Mora, "Battery-assisted and photovoltaic-sourced switched-inductor CMOS harvesting charger-supply, " *IEEE Int. Symp. Circuits Syst.*, pp. 253-256, May 2013.

115. S. Kim and G. A. Rincon-Mora, "Dual-source single-inductor 0.18μm CMOS charger-supply with nested hysteretic and adaptive on-time PWM control, " *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 400-401, Feb. 2014.

116. S. Kim and G.A. Rincon-Mora, "Single-inductor fuel cell-li ion charger-supply IC with nested hysteretic control, " *Analog Integrated Circuits and Signal Processing Journal*, vol. 70, no. 1, pp. 33-45, Jan. 2012.

117. S. Kim and G.A. Rincon-Mora, "Achieving High Efficiency under Micro-Watt Loads with Switching Buck DC-DC Converters, " *Journal of Low-Power Electronics*, vol. 5, no. 2, Aug. 2009.

118. D. Kwon and G.A. Rincón-Mora, "Operation-based signal-flow ac analysis of switching dc–dc converters in CCM and DCM, " *IEEE Int. Midwest Symp. on Circuits and Syst.*, pp. 957-960, Aug. 2009.

119. Y. Wang, Y. Huang, P. Huang, H. Chen and T. Kuo, "A Single-Inductor Dual-Path Threee-Switch Converter With Energy-Recycling Technique for Light Energy harvesting," *IEEE J. of Solid-State Circuits*, vol. 51, no. 11, pp. 2716–2728, Nov. 2016.

120. R.D. Prabha and G.A. Rincon-Mora, "How to Design Battery-Assisted Photovoltaic Switched-Inductor CMOS Charger–Supplies," *IEEE Int. Symp. Circuits Syst.*, May. 2017.

121. G. Yu, K.W.R. Chew, Z.C. Sun, H. Tang and L. Siek, "A 400nW Single-Inductor Dual-Input-Tri-Output DC-DC Buck-Boost Converter with Maximum Power Point Tracking for Indoor Photovoltaic Energy Harvesting," *IEEE J. of Solid-State Circuits*, vol. 50, no. 11, pp. 2758–2772, Nov. 2015.

VITA

RAJIV DAMODARAN PRABHA

Rajiv Damodaran Prabha received B.Tech degree from National Institute of Technology Calicut, India in 2007, and M.S. degree from Georgia Institute of Technology, Atlanta, GA, USA, in 2011, respectively, both in electrical engineering. He did his Ph.D. degree at Georgia Institute of Technology. His research interests include energy harvesting circuits, switching power supplies and, other power and performance analog circuits. He is currently working as an analog design engineer in the power interface group for Texas Instrument Inc. Manchester, NH.